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DESIGN OF ENERGY EFFICIENT HYBRID 1-BIT FULL ADDER FOR ARITHMETIC APPLICATIONS

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***Abstract*— This paper presents an energy efficient 1-bit full adder designed with a low voltage and high performance internal logic cells which leads to have abridged Power Delay Product (PDP). The customized XNOR and XOR gates, a necessary entity, are also presented. The simulations for the designed circuits performed in cadence virtuoso tool with 45-nm CMOS technology at a supply voltage of 0.9 Volts. The proposed 1-bit adder cell is compared with various trendy adders based on speed, power consumption and energy (PDP). The proposed adder schemes with modified internal entity cells achieve significant savings in terms of delay and energy consumption and which are more than 77% and 40.47% respectively when compared with conventional "C-CMOS" 1-bit full adder and other counter parts.**

Keywords— VLSI, high speed, energy efficient, hybrid full adder.

I. INTRODUCTION

The demand and reputation of handy electronics is motivating designers to strive for lesser silicon area, lower delays, longer battery life, and more consistency. For any system, power consumption can be reduced by scaling the supply voltage and operating frequency. Whereas, it increases the propagation delay of the circuit and which in turn degrade the driving capability of the entire design [1-2]. In recent days a novel low power hybrid adders have introduced for on-chip communications, which works with smaller amount of energy for its operation. In the field of communication, energy efficient computing will play a vital role to maximize the circuit performance when we operate the device at sub threshold or near threshold regime [3-4]. The "Built In Self Test (BIST)" is a most suitable application in communication system for its counter and minimizing error analysis using CMOS sub-micrometer, so as to attain smaller chip size with lofty operating speeds and efficient usage of energy. Therefore it is a new trend setter in the field of communication for computing applications [5]. The rest of the paper is organized as follows: Section 2 describes literature survey and proposed circuit implementation is introduced in section 3. Section 4 presents the result and discussion. Section 5 draws the conclusion.

II. LITERATURE REVIEW

The power expenditure is a most important concern for emerging appliance like smart phones, smart cameras, multimedia processors, etc. The power expenditure can diminish by number of approaches. The "Multiple Supply Voltage" (MSV) design is a prevailing technique for the diminution of power consumption of System on Chips (SoCs). The SoCs uses Voltage Level Shifters (VLSs) and the VLSs would become overhead while its own power expenditure & circuit delay is high. The VLSs become efficient with feedback network to remain the output voltage stable at all possible loading conditions. Robustness of the VLSs can be examined at high frequencies with standard unit of loads with elevated temperature. The VLS are the key interfacing components in all most all SoCs in recent days [6].

The CMOS Current limiters are more practical electronic circuits having a provision of current limit for different loads with the provision of preventing the design to generate and transmit higher current levels for unsafe effects due to any short circuit or no load. The most common current-limiters are realized to have a voltage drop from too high to low voltage supply rails. In practical cases, where the power rail voltages need the in-house current-limiters, they are habitually built using current sensors, current control circuits and pass transistors. The double level current limiters are more predominant to achieve low power consumption with nanosecond delays [7].

Ebrahim Pakniya et.al. [8] proposed a design "energy efficient 16T FA cell for near-threshold voltage technology". This paper focused about two new structures of one - bit full adder circuits suitable for sub-threshold voltage. Comparison has been carried out for propagation

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delays, power dissipations, PDP, and EDP in sub threshold regime.

To decrease the overall "power consumption" and "propagation delay" a new full adder scheme is designed with internal logic cell. This logic cell employed with XOR/XNOR gates, multiplexers inserted at the output with modified universal gates. The sum and output carry is selected with the help of Multiplexers. Proposed design has full output swing and is found suitable when operated at lower voltages to maximize the energy efficiency.

III. PROPOSED METHOD

The internal logic cell depends on transmission function theory is presented to develop the 1-bit full adder cell as shown in below figure 1. It consists of three core blocks to achieve the output sum and carry. This arrangement has been adopted by a lot of researchers as a benchmark structure for developing the 1 bit full adder cells. The basic approach to realize the "exclusive OR" and "exclusive NOR" (XOR/XNOR) functions is to synthesize the XOR gate and produce the XNOR gate with the help of inverter.

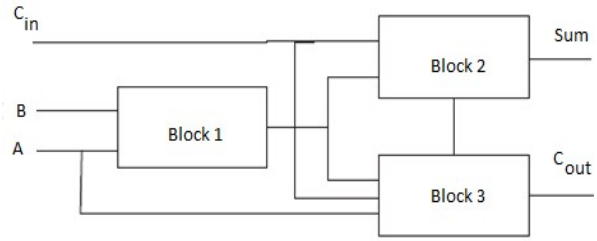

Fig.1. General form of XOR–XNOR-based full adder

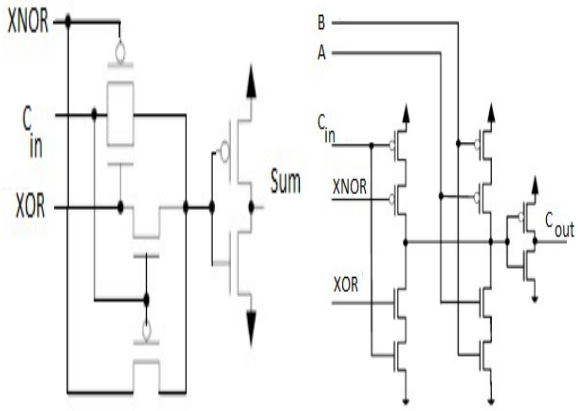

Fig.2. Circuit diagram of Block 2 and Block 3

The circuit shown in figure 2, which corresponds to block 2, guarantees the sufficient drive to cascaded scheme with the help of inverter. On the other hand, the circuit scheme which is employed by complementary "C-CMOS" logic style is shown in figure 2 which corresponds to block 3. Propagation delay of the proposed design is minimized by sizing the XOR/XNOR, customized AND/OR gates and multiplexers. The sizing of the transistors is also supportive to decrease the glitches in cascaded applications. The circuit diagram of proposed "Hybrid Full Adder" (HFA) for generation of carry and sum are shown in figures 3 and 4 respectively. The post layout simulation waveforms of XNOR circuit and proposed HFA circuit are shown in figures 5 and 6 respectively.

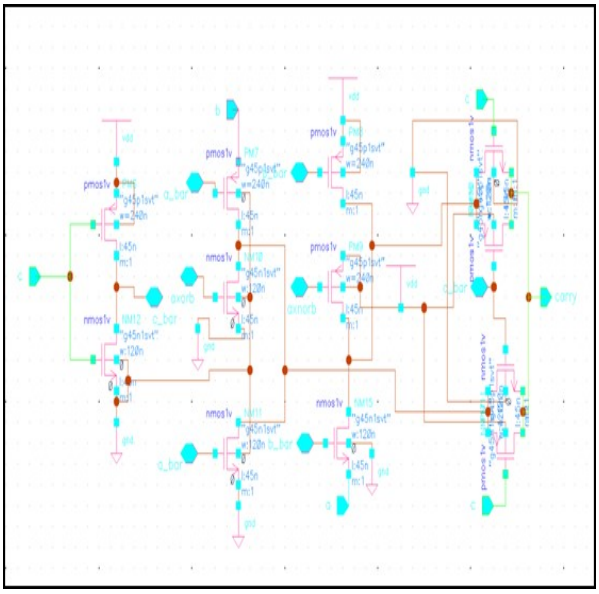

Fig.3. Circuit diagram of proposed HFA carry circuit

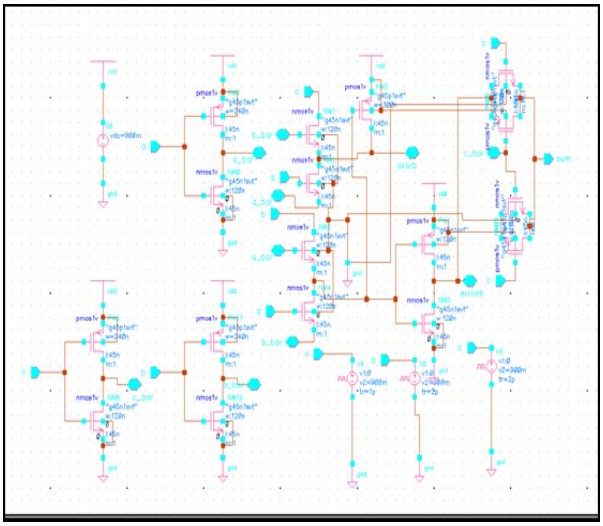

Fig.4. Circuit diagram of proposed HFA sum circuit

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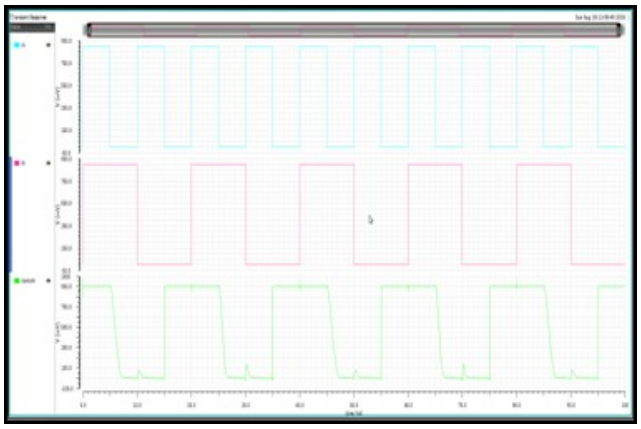

Fig.5. Post layout wave form of XNOR circuit

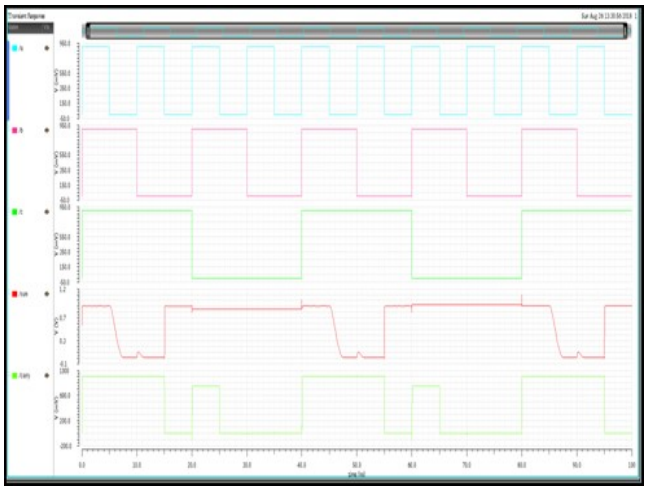

Fig.5. Post layout wave form of proposed HFA circuit

IV. RESULTS AND DISCUSSION

Simulation results of different full adder circuits at 0.9 Volts are shown in Table 1. The graphical analysis of various 1-bit full adder circuits in terms of delay, power and PDP are depicted in figure 6. The simulations for the proposed HFA circuits are performed in cadence virtuoso tool with 45-nm CMOS technologies at a supply voltage of 0.9 Volts. The proposed HFA circuit achieves more than 76%, 68% and 40% delay as compared to C- CMOS and other counter parts. Similarly, the PDP of 71%, 55% and 30% as compared to C- CMOS and other counter parts at cost of average power consumption.

TABLE1. SIMULATION RESULTS OF DIFFERENT FULL ADDER CIRCUITS AT 0.9 VOLTS

FA Design	Power (uW)	Dealy (ns)	PDP (aJ)
C-CMOS	0.256	0.1309	33.51
Hybrid	0.231	0.094	21.71
Hybrid CMOS	0.268	0.0521	13.96
Proposed	0.3206	0.03	9.618

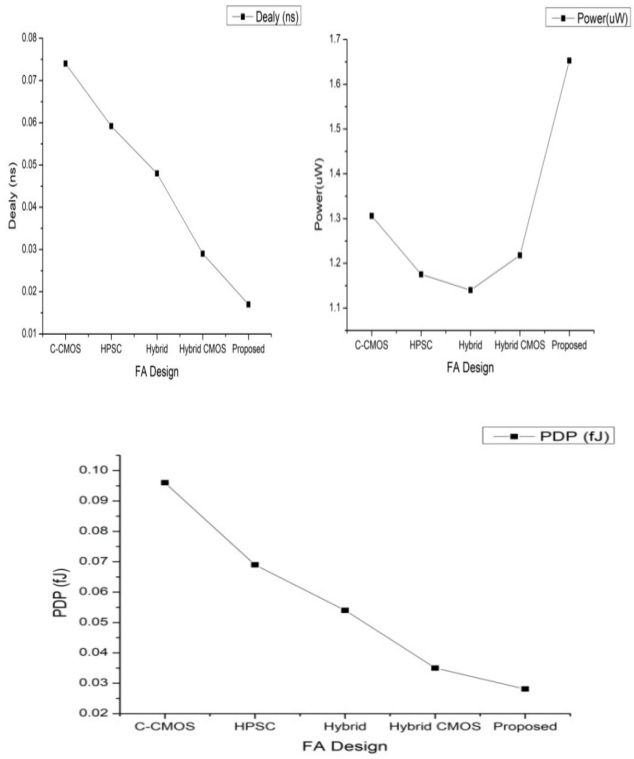

Fig .6. Performance metrics of different full adder designs at 0.9 Volts

V. CONCLUSION

In this paper, l-bit HFA circuit is presented depends on energy efficient internal logic cells. All the simulations are carried out on cadence tool by using 45-nm technologies to estimate the proposed design and existing designs. From the results it has been observed that the design has lowest delay and minimum PDP when compared to numerous existing adder circuits. Subsequently, the proposed HFA is set up suitable choice

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at low operating voltages with full swing output. The proposed adder schemes with modified internal entity cells achieve significant savings in terms of delay and energy consumption and which are more than 77% and 40.47% respectively when compared with conventional “C-CMOS” 1-bit full adder and other counter parts. From the performance point of view, it clear that, the design might be a choice in the upcoming nanoscaling applications.

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