

Estimation of Leakage Power and Delay in CMOS Circuits

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Abstract—This paper presents an estimation of leakage power and delay for 1-bit Full Adder (FA) designed which is based on Leakage Control Transistor (LCT) NAND gates as basic building block. The main objective is to design low leakage full adder circuit with the help of low and high threshold transistors. The simulations for the designed circuits performed in cadence virtuoso tool with 45 nm CMOS technology at a supply voltage of 0.9 Volts. Further, analysis of effect of parametric variation on leakage current and propagation delay in CMOS circuits is performed. The saving in leakage power dissipation for LCT NAND_HVT gate is up to 72.33% and 45.64% when compared to basic NAND and LCT NAND gate. Similarly for 1-bit full adder the saving is up to 90.9% and 40.08% when compared to basic NAND FA and LCT NAND.

Keywords—Leakage Control Transistor, NAND Gate, Adder, Leakage Power and Delay.

I. INTRODUCTION

The CMOS technology has experienced aggressive scaling over the last 40 years driven by the benefits of enhanced integration density, speed of operation and power dissipation. To increase the performance of the circuits and to integrate more functions into each

chip, feature size has to continue to shrink. Because of the hostile advancements in VLSI technology (scaling of feature size) integration capacity of IC is rises. Which intern improves the processing speed of IC, but it also increases the power dissipation and temperature of IC [1].

Leakage power dissipation is eventually becoming comparable to dynamic power dissipation in many high performance designs when the design is at near threshold computing applications. The very large level of integration results in complication of heat removal; this in turn increases the cost of cooling and packaging [2].

Self Controlled Stacked Transistor (SCST) or Leakage Control Transistor (LCT) technique is the technique to reduce leakage power consumption in CMOS gates without affecting the dynamic power of the circuit [3-4].

In this paper, various NAND gates with low and High threshold transistors are proposed to design an energy efficient arithmetic circuits for computing applications. The rest of the paper is organized as follows: Section 2 describes literature survey and proposed circuit implementation is introduced in

section 3. Section 4 presents the result and discussion. Section 5 draws the conclusion.

II. LITERATURE REVIEW

M. Mahaboob Basha et al., implemented LFSR counter analysis using CMOS sub-micrometre, so as to achieve lesser chip size with high operating speeds and to maximize the energy utilization [5].

G. Srinivasulu et al., proposed current limiters based level shifters for IOT applications. Most universal current-limiters uses voltage drop mechanism from too high to low-voltage supply rails. In general, inner current-limiters are usually constructed using current sensors, pass transistors, and control circuits. Current sensors are uncomplicated low valued resistors, are built-up with transistors and voltage across would be proportional to that of current, the low valued resistors poses static current, leads static power in the circuit [6].

Multi voltage clustered structures are the fundamental and imperative power lowering techniques; utilize voltage Level shifter (LS) circuits to intercommunicate “Multiple voltage circuit blocks” to shrink power at core or circuit modules. The LS may deem as delay and power expenditure when its individual contributions are high. The developed Diode current limiter LS have implemented in 130nm technology, which minimizes power and delay at the cost of area overhead [7].

Optimization at the logic level can be achieved by minimizing the logic by its equivalent and Boolean based logic reduction, logic level power down alike. Logic level power down controls the

logic switching activity at the expense of additional circuits. Optimization depends on the circuit complexity and other factors at this level. Up to 50% power consumption can be possible with these methods. Pass transistor based MOS Switch Integrated Ultra Low Power 1-bit full adder (MOSSI-ULP) is the design by Vijayakumar and Reeba Korah for which the biasing techniques are applied to restore the full swing [8].

Y. Amar Babu et.al., proposed [9] a novel area and power efficient on chip communication architectures for image encryption and decryption using single soft processor (Micro Blaze). Proposed System On Chip explores On chip Communication architectures features to efficiently implement the application. The SoC offers scalability and guarantees on the timing behaviour when communicating data between various processing and storage elements. Proposed SoC has been implemented on Spartan6 FPGA and evaluated at 83.33 MHz. It has occupied only 19% of resources available on target FPGA, consumes very low power 68 mW, 15% of conventional architectures. The proposed on chip communication architectures compared with device utilization on FPGA and power consumed.

Dynamic threshold transistors are used to reduce the propagation delay within the given leakage power consumption constraints. The performance metrics like power, delay, Energy and Energy Delay Product (EDP) were evaluated by varying the threshold level of a transistor dynamically at ultra-low supply voltages [10].

Various energy efficient arithmetic circuits at low supply voltages and ultra-

low supply voltages have been proposed by various authors namely adder, multipliers, subtractor, divider and level shifter in the literature [11-16]. From the literature it has been clear that power and delay are the two performance metrics which can decide the energy metric of a digital circuit in low power applications.

III. PROPOSED METHOD

For MOS transistors in deep submicron technology subthreshold current varies exponentially with gate-source voltage (V_{gs}) of the transistor. In CMOS circuits, very minor current drifts even at $V_{gs} = 0$ volts and is known as leakage current.

Furthermore, the CMOS logic circuits are employed with series-parallel network of p-channel and n-channel transistors. Dual threshold transistors are used to reduce the leakage power consumption within given delay constraints.

Leakage Control Transistors (LCT) used in self-controlled stacked transistor technique are replaced by transistors having high threshold voltage. LCT based two input NAND gate circuit is shown in figure 1.

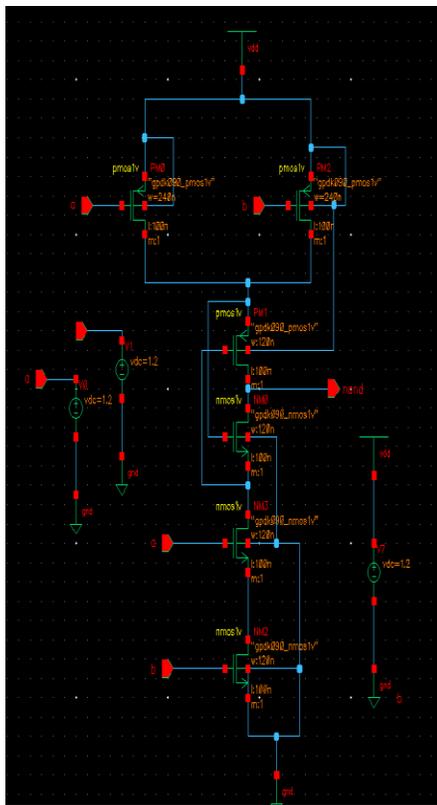


Fig.1.Circuit diagram of LCT NAND gate

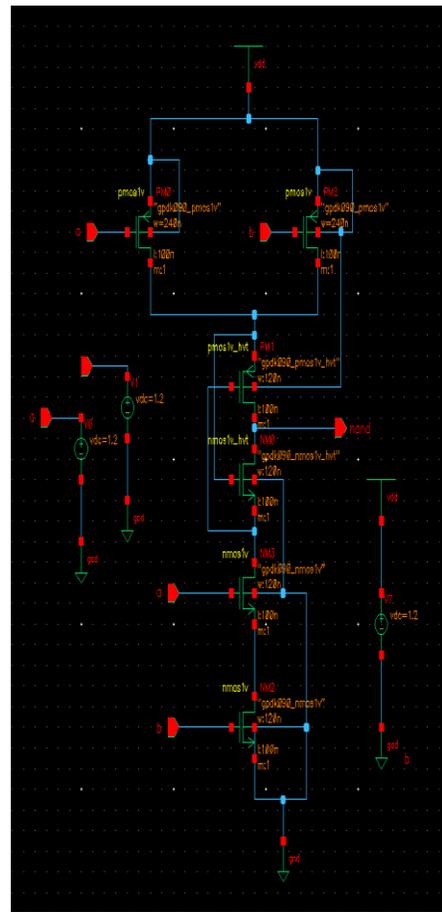


Fig.2.Circuit diagram of LCT NAND_HVT gate

Here, M1 and M2 as leakage control self bias stack transistors where the Gate of p-channel and n-channel MOSFET is connected to the drain terminal of n-channel and p-channel MOSFET respectively. Modified NAND gate with threshold transistors M1 and M2 represents the application of high threshold transistor technique which is shown in figure 2.

Here, one of these two transistors are always operates in its cutoff region. The outcome of this technique is an increase of number of OFF transistor from supply voltage to ground path and consequently increasing stack effect.

The benefit of both high threshold and stack effect is employed to decrease power consumption.

IV. RESULTS AND DISCUSSIONS

Initially the conventional NAND and LCTNAND logic in 45nm technology were simulated as they are the basic block for any digital systems, then the simulation has been carried out for proposed LCTNAND_HVT shown in table 1. Based on the above 3 different NAND gates a 1-bit full adder was proposed.

The simulation results of proposed adder along with conventional and LCTNAND based adder were shown in table 2. From the results it has been clear that the average leakage power for the proposed design is less both in case of NAND gate as well as NAND gate based 1-bit full adder.

Reduction of leakage current is the predominant factor when the circuits are operated at ultra-low voltage application as compared to dynamic power consumption. The graphical analysis of various designs related to NAND circuits

in terms of average leakage power is depicted in figure 3 and figure 4 shows the average leakage power of different full adder designs.

TABLE I
SIMULATION RESULTS OF VARIOUS NAND GATES

Design	Average leakage Power (nW)	Average total Power (nW)	Delay (ps)
NAND	1.059	112	9.5
LCT NAND	0.539	148	23.8
LCT NAND_HVT	0.293	128.3	48.8

TABLE II
SIMULATION RESULTS OF VARIOUS FULL ADDERS

Design	Average Leakage Power (uW)	Average total Power (uW)	Sum Delay (ns)	Carry Delay
NAND based FA	3.251	2.582	0.1265	0.068
LCT NAND based FA	0.494	4.268	0.3402	0.181
LCT NAND_HVT	0.296	15.97	0.4301	0.221

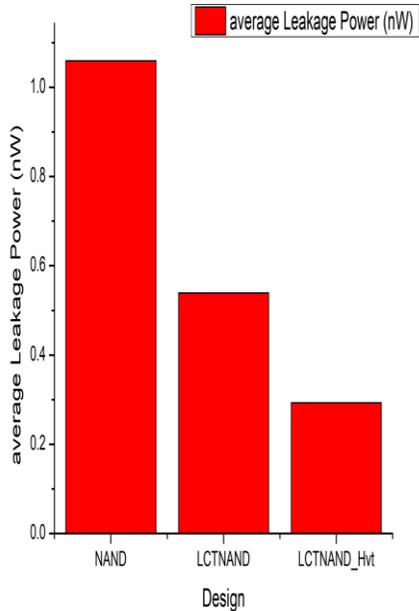


Fig.3. Average leakage power comparisons of various NAND designs

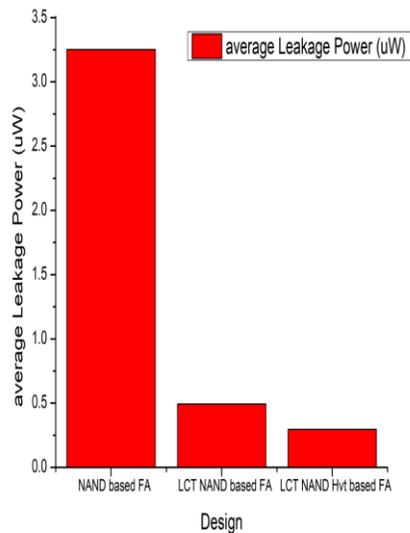


Fig.4. Average leakage power comparisons of various full adder designs

V. CONCLUSIONS

Various NAND gate designs are investigated to minimize the leakage power as well as average power with the help of LCT and HVT approaches. Based on the basic NAND gate and the proposed NAND gate, a 1-bit full adder is implemented.

Leakage power consumption is measured by stimulating the circuits with the same set of input vectors at 45-nm process technology and various parameters are obtained for the analysis of the circuits. Power is measured and average is done for all the input vectors to attain the average leakage power dissipations.

From the simulation results, by comparing with basic NAND and LCT NAND based full adders, the proposed HVT NAND based full adder is better in terms of average leakage power. The saving in leakage power dissipation for LCT NAND_HVT gate is up to 72.33% and 45.64% when compared to basic NAND and LCT NAND gate. Similarly, for 1-bit full adder the saving is up to 90.9% and 40.08% when compared to basic NAND and LCT NAND FA.

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