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A Novel Decimal Arithmetic Operations By using FPGA Logic Block Architecture

Ms. C. Mythile[1], Mr. A. Basheeth[2] , Mr. R. Logarasu[3]
[1]*UG –Applied Electronics, Selvam College of Technology, Namakkal, Tamilnadu.*
[2]*Associate Professor, Department of Electronics and Communication, Selvam College of Technology, Namakkal, Tamilnadu*
[3]*Associate Professor, Department of Electronics and Communication ,Selvam College of Technology,Namakkal, Tamilnadu*

ABSTRACT
To improve the efficiency of decimal computation functions in Field-Programmable Gate Array (FPGAs) are used by Hardened adder and carry logic. There are many design choices and complexities associated with such hardening, FPGA architectural choices, power consumption. Moreover, those choices have not been studied much and hence i explore a number of possibilities.For avoiding inaccuracy, introduced when converting fragment of numeric to double, these data are processed with decimal computation operation. Most processors only have hardwired double computation units. So, decimal operations are executed with slow software decimal computation functions. For the fast output of decimal operations, devoted tackle units have been proposed and designed in Field Programmable Gate Array.Compared to former architectures, my perpetration results show that the proposed computation operations achieve 15 percent better area and 12% better performance.

Keywords—Hardened adder, Field- Programmable gate array (FPGAs), Look up table(LUT), Xilinx.

1. Introduction

Field Programmable Gate Arrays (FPGAs) combine limited cost and reconfigurability with veritably high make in to one unit installation and performances. Similar characteristics, along with reduced price and make them a valid alternative to the further multifold and time to market demanding Application Specific Integrated Circuits (ASICs) Sum of digit is the main operation of each computation circuit, thus improving speed performances and reducing the area occupancy of adder circuits is still an initiative research topic .

The existing adder structures similar as Ripple Carry Adder (RCA), Carry Look Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSEL), Carry Bypass adder (CBY) and Area Effective Carry Select Adder (AECSA) are verified based on the performance. Among all structures, some structures reduce the area occupied by the circuit with the increased detention and some structures reduce the detention with the increased consumption of area. The proposed adder structure results in optimized performance, that is, the detention is reduced with the equal consumption of area which was observed in normal adder design. The characteristics of the digital circuit are anatomized substantially grounded on the time and area consumption. Programmable gate arrays give an alternative approach to application specific integrated circuits (ASIC) implementation with features like large-scale integration, design verification post production,

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lower non-recurring costs, reconfigurable design approach etc. [11]

Field Programmable Gate Arrays (FPGAs) combine limited cost and reconfigurabilitywith high integration capability and performances. Such characteristics, along with reduced low volume costs make them a valid volition to the more complex and time to vend demanding Application Specific Integrated Circuits (ASICs). [8] Addition is the main operation of each calculation circuit, therefore perfecting speed performances and reducing the area occupancy of adder circuits is still an enterprising research topic. Unfortunately, as it is well known, designing effective adders using an FPGA platform is not trivial. [6] These blocks are highly optimized in terms of speed or area thereby facilitating efficient realization of complex functions .One of the major changes in the FPGA has been the preface of 6-input LUT as a basic element .

With this FPGA primitive, the sense perpetration would lead to advanced sense consistence performing in a minimal-depth circuit and advanced speed - a trend towards which the current FPGAs are acquainted. Maybe the biggest issue with 6-input LUTs is their under application while implementing a particular sense function, since numerous functions do not bear six inputs where FPGA more effective, if the function occurs frequently in applications, and there is a large advantage when it enforced in hard, rather than soft sense. As adder-type computation functions appear frequently and hardened adders important faster than soft adders, commercial devices commonly have hardened adder and/or carry logic and routing.

2. PROPOSED METHODOLOGY

The suggested solution uses a foundation soft logic block with hardened adder and carry chains to create a 1 bit adder and a 4 bit carry look aheadadder. Each BLE is made up of LUT and a flip-flop with rapid feed forward and feedback channels that are similar to those seen in FPGAs. As a result, a mux may be employed, although the circuit latency may vary greatly depending on the circumstances. Each FLUT in the FLUT design may provide two separate outputs. This allows for the inclusion of a second bit of addition in FLUT at a low cost. The balanced 2-bit adder, in contrast to the balanced 1-bit adder FLUT on the left, demands that each 5-LUT be further fractured down into two 4-LUTs with the most input shared, in order to give the adder with the requistic four addends.To reduce carry propagation of addition, a decimal adder was devised that considers an excess-5 representation.

To implement the adder, this adder is utilised in the suggested multipliers. It also serves as the foundation for a novel decimal adder, which is required for the partial product generators' design.The circuit for a single digit of block of computation decimal operations with a carry-in and a carry-out is created by connecting these propagate and generate signals with a carry chain. The hardening of adders and the carry chain improves the performance of decimal computing operations and reduces circuit latency. As a result, the flip-flop is employed, but the timing summary in the implementation synthesis is modified. It outperforms the existing technique by 15% and 12% in each of the areas.

Though it is obtained through low-level operations, the inputs were characterised as a set procedure. If A=0, then B=0 is the output. Similarly, in the complete adder, state-of-the-art is defined. Sum values and carry-out flags were the conclusions obtained in terms of output values.

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This result is based on the assumption that the operational power consumption would be high in order to attain the predicted logic value.

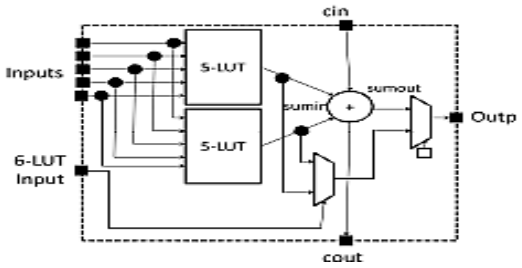

Fig 1.Proposed Architecture.

The FA is established using two LUT6-1s. [3] LUT6-1 is a slice-wide basis LUT. Because the sum value and carry-out flag can be implemented simultaneously, two basic LUT6-1s are utilised, one for the Sum circuit and the other for the Carry-out circuit. The two truth tables of addition, as well as the circuits of the Carry-out flag for addition. It has been discovered that they may be combined to produce FA/S with control=0, Furthermore, the final circuit for FA is created by dividing a single LUT (6 input, 2 output) into two little LUTs, one for Sum and the other for Carry-out flag. When the Carry-out flag is set to 1, the result is 'overload.' As a result, the Sum/Sub and Carry-out flags can both run simultaneously.

Unlike the well-known ripple-carry design, which has a total time delay proportionate to the length N of the adder, the carry look ahead design allows extra logic circuitry to create all carries concurrently. [14]. As a result, regardless of the length of the adder, the adding time remains constant. For a better grasp and a quick overview of this adder type's logical structure.

If the CLA unit can be arbitrarily enlarged, it is theoretically conceivable to design adders of any word length. In reality, however, the CLA unit's complexity is constrained. A hierarchical structure based on Block-Carry-Look-Ahead (BCLA) units results. Adaptive structure creation, technology mapping, partitioning, and placement are the four processes in the construction of hierarchical CLA adders. I show implement all of these stages in any SRAM-based FPGA that can be characterised by the generic models given.

3. Results and Discussion

3.1 Xilinx

Xilinx ISE (Integrated Synthesis Environment) is a discontinued Xilinx software tool for synthesis and analysis of HDL designs, with a focus on VLSI development. The "X" denotes programmable logic pieces at each location. The "Linx" stands for the programmable linkages that connect the logic pieces.

Its partial reconfiguration approach lets designers to modify functionality on the fly, reducing the need to completely reconfigure and reestablish connections, greatly increasing FPGA flexibility.ISE allows programmers to synthesise (or "compile") their designs, do timing analysis, analyse RTL diagrams.

To simulate a design's response to various stimuli, and configure the target device with the programmer. Xilinx ISE is strongly connected to Xilinx's own chip design (the internals of which are highly confidential) and cannot be utilised with FPGA devices from other vendors. It's generally

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used for circuit synthesis and design, whereas system-level testing is done with ISM, or the Modelsim logic simulator.

S.No	Parameters	Existing Method	Proposed Method
1.	Slice Lut	28	20
2.	Combinational Delay in ns	6.485	6.425
3.	Power in Watts	0.041	0.023
4.	Area Efficient	25%	12%

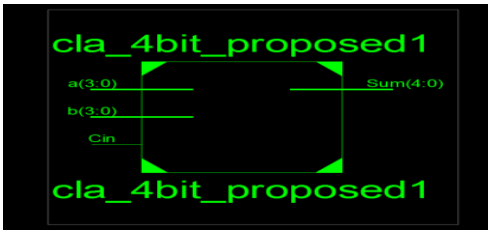

Fig.2. Proposed Output

CONCLUSION

The purpose of this paper is to propose a new FA architecture on an FPGA platform with two optimization goals. The first is to improve the FA/S ratio in order to increase speed. The second is to create a new circuit for FA/S to allow for production with fewer gates. As a result, the proposed design is based on the multiplexer and contains only two types of components: NOT gate and multiplexer, allowing the design to be easily implemented on an FPGA chip.Both designs are subjected to detailed testing using different FPGA series. The experiment revealed that the proposed n FA performed 20% to 30% faster than the standard FA using the same area resources, and the proposed n FAS performed 28% to 40% faster than the standard FA/S using only half the resources.

- If the expression is true , the statements inside the if block will be executed.
- If the expression is false, the statement inside the if block will not be executed.

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