International Journal of Engineering Technology and Management Sciences
Website: ijetms.in Special Issue: 1 Volume No.7 April – 2023
DOI:10.46647/ijetms.2023.v07si01.011 ISSN: 2581-4621

Design a CMOS Flash ADC Architecture With Low Power and High Speed Operation

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Abstract
Analog-to-digital converters (ADCs) are essential to the present digitized world because they process analog signals. Several embedded, communication, and signal processing systems make use of ADCs. In this study, a high speed, low power CMOS flash ADC architecture is shown. The proposed architecture is implemented using 180 nm CMOS technology. The principle of most significant bit (MSB) creation is employed with a switching reference voltage. A low power TIQ comparator has been used to generate the range of reference voltages. The reference voltage is switched by a control circuit at the halfway voltage of the input signal (Vk). The current architecture uses 2^{N-1} comparators as Compared to the 2^{N}-1 comparators of a conventional flash ADC. The recommended flash ADC also has a low power encoder. The circuits are designed using TANNER EDA and the performance is analyzed with a total power consumption of 595.78µW with an input signal frequency of 1GHz.
Keywords— *Flash ADC,TIQ Comparator, CMOS ROM, Comparator, Control Circuit.*

I. INTRODUCTION

ADCs are essential in today's digital world because they convert analog signals to digital signals. Both as stand-alone components and as the foundation of more complicated systems, ADCs are crucial [1]. Because to the advancement of new fabrication techniques, almost the entire system, including the ADC, may now be combined on a single chip. The applications of ADC are expanding quickly in a variety of fields, including the Internet of Things (IoT), information-on-demand, embedded system devices, signal processing, and communication, in accordance with the concept of system-on-chip (SOC) [2]. To satisfy the crucial requirement of low power consumption, mixed-signal integrated circuits must be built with constrained energy, a suitable size, and minimal power dissipation [3]. There are numerous ways to alter an analog signal.

It is challenging to create a rapid, low-power ADC design. According to multiple researchers who have devised and recommended various methods, it is possible to reduce the amount of power used, the amount of space required, and the delay. For a power-saving architecture that allows only half of the comparators to function during each clock cycle, the bisection approach is suggested [4]. A two-step ADC has been developed using a voltage estimator. This method reduces both the die size and power consumption in half [5]. To achieve the best speed while consuming the least amount of power, a time-interleaved multi step ADC has been implemented [6]. Flash ADC multiplexes create reference voltages to conserve energy and use fewer comparators [7].

The power, size, and delay of the flash ADC have recently decreased thanks to a wide range of specialised architectures. In place of the 2^{N} - 1 comparators utilised in the traditional flash ADC, comparators are necessary in the proposed flash ADC architecture (where N is the number of bits). The current design, as opposed to the bisection approach [4], multi step ADC designs [5]–[6], or multiplexer-based architecture [7], generates the most significant bit (MSB) with a switched reference voltage. Where as the other bits are formed using an automatically changing reference voltage, the MSB is produced using a single comparator in accordance with the input signal. A comparator used to create MSB is built using the Threshold Inverter Quantization (TIQ) technique to reduce power consumption and architecture complexity.

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II. LITERATURE SURVEY

In this project, we did a survey on Chia-Chun Tsai, Kai-Wei Hong, Yuh-Shyan Hwang, Wen-Ta Lee and Trong-Yen Lee[4] was proposed a 6 bit New power saving design method for CMOS flash ADC. In this paper flash ADC is presented with an inverter as a comparator along with an NMOS and PMOS as switches, in this paper the authors used bisection method to let only half comparators in flash ADC working in every clock cycle. The proposed ADC operates at 200MHz sampling rate and 3.3V supply voltage. The power consumption of the circuit is 40.75mW.

III. EXISTING METHOD

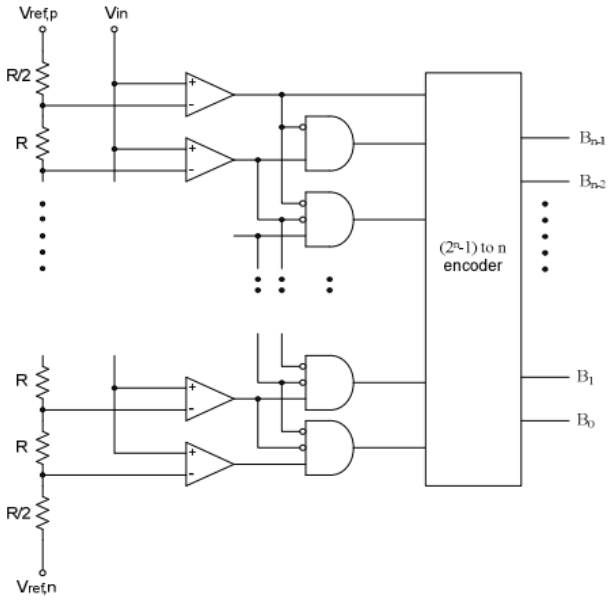

Fig. 1. Block diagram of n-bit flash ADC

"Fig 1" represents a block diagram for an n-bit flash ADC. An essential component of the majority of electronics and communication systems nowadays is an analog-to-digital converter (ADC). The comparator is the key component in analog to digital conversion (ADC). The reference voltage is a set of 2N reference voltages. These voltages are compared to the analog input signal in just one clock cycle. At this point in the ADC process, the signal is essentially transferred from the analog to the digital domain. The Flash ADC is the fastest of all the numerous ADC designs that are available. An N-Bit Flash ADC converts data using 2^N-1 comparators. Yet, these comparators consume a lot of power because they run in parallel.The converter needs a lot more power because the Flash ADC additionally needs a resistor ladder circuit or capacitor array circuit to supply reference voltage . The Flash ADC utilises the most power out of all the different kinds of ADCs as a result. One of the main limitations for low power data conversion circuits has been found to be power dissipation. Power efficiency is actually a key design objective for many battery-powered applications, such as pacemakers, wireless sensor nodes, and other implanted RFID chips used as biomedical imaging devices in the human body . The objective in these circumstances is to extend battery life while consuming the least amount of power possible. The 6-Bit Flash ADC employed in this study satisfies the requirement.

IV. PROPOSED METHOD

"Fig. 2" depicts the architectural layout of the suggested flash ADC. In contrast to the standard flash ADC, which requires 2^N-1 comparators, the implementation of the N-bit suggested flash ADC design only requires 2^{N-1}. The TIQ comparator, CMOS inverter, 5-bit conventional flash ADC, and control circuit are the key components of the schematic diagram for the proposed 6-bit flash ADC. A two-stage open-loop comparator pair, NAND logic, and CMOS ROM binary encoder make up a 5-

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bit conventional flash ADC. The next subsections illustrate the design and analysis of the building blocks.

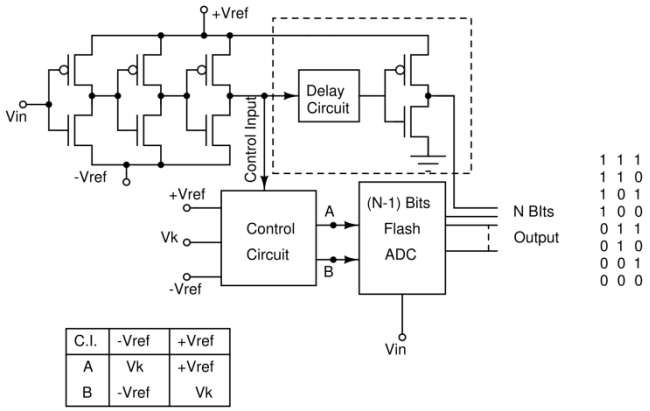

Fig. 2. Architecture of Proposed Flash ADC

The suggested ADC architecture consists of two separate parts that together make up the digital output code. Segment one, which corresponds to the MSB, is formed by a single comparator, as can be seen in "Fig. 3". Equation 1 illustrates how switching reference voltages at the midway voltage (Vk) in relation to the input signal voltage generates the remaining bits in segment two automatically.

$$Vk = \frac{(+Vref)+(-Vref)}{2} \qquad (1)$$

Where +Vref is the input signal's maximum range and -Vref is its minimum range. When Vin <VK, the reference voltage to the flash ADC will be taken into account as VK to -Vref. Similar to this, when Vin > VK, the flash ADC will use +Vref to VK as the reference voltage. The MSB (either zero or one) is generated in both scenarios using a single comparator in accordance with the input signal voltage.

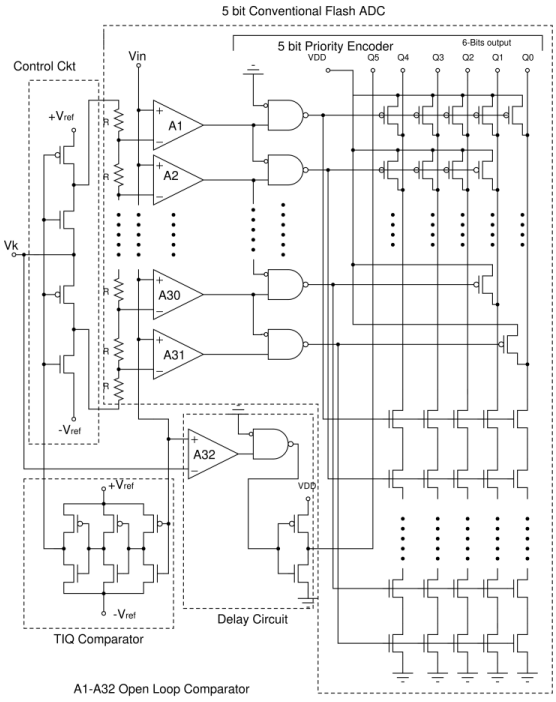

Fig. 3. Schematic Diagram of Proposed 6-bit Flash ADC

A. Control unit

The control circuit's circuit diagram is shown in "Fig. 4". This circuit, which is an essential component, provides the resistive divider network with an automatically switched reference voltage that depends

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on the input signal. A comparator compares the voltages present at each node of the resistive divider network to the analog input voltage Vin. Because all resistor values are equal, the two reference voltages, +Vref and -Vref, divide the available voltage levels at the nodes equally. The resistive divider network provides each comparator with a unique input reference, where RL denotes the resistors' series arrangement. The control circuit generates the reference voltage across the load resistor in accordance with the control input.

A control circuit is designed to give an automatically switched reference voltage, as shown in "Fig. 4". The comparator initially compares the input signal to the threshold before creating the appropriate control input. If Vin > VK, the control input will be logic high, and if Vin <VK, it will be logic low. The reference voltage is generated by the control circuit from VK to -Vref in the event of a logic high and from +Vref to VK in the event of a logic low, as shown in "Fig. 11". The control circuit also uses two identical inverters with equal-sized threshold voltages, as seen in "Fig. 4".According to the control input, the control circuit produces the reference voltage across the load resistor.

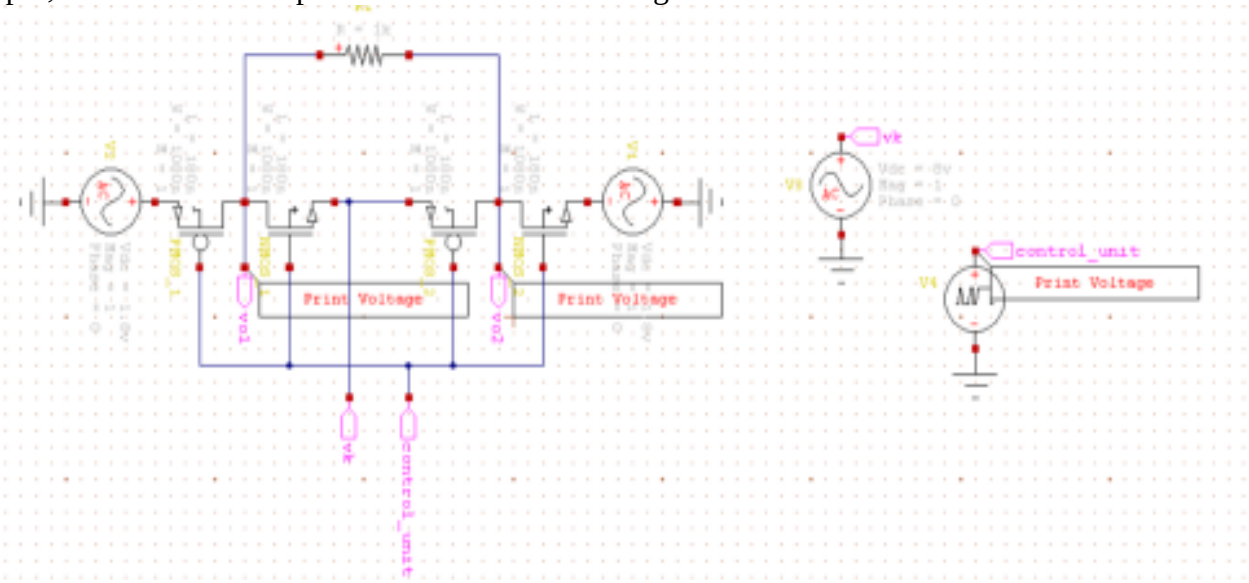

Fig. 4. Control Circuit

As seen in "Fig. 4", a control circuit is created to provide an automatically switched reference voltage. Before providing the appropriate control input, the comparator first compares the input signal to the threshold. The control input will be logic high if Vin > VK and logic low if Vin <VK. According to "Fig. 4", the control circuit generates the reference voltage from VK to -Vref in the event of a logic high and from +Vref to VK in the event of a logic low. As shown in "Fig. 4", the control circuit also employs two identical inverters with comparable threshold voltages.

$$\frac{K_N}{K_P} = \left(\frac{|V_{ref}|+V_{thp}-|V_{th}|}{|V_{th}|-V_{thn}}\right)^2 \qquad (2)$$

A CMOS inverter's ratio of the NMOS and PMOS trans-conductance characteristics can be expressed as "(2)" [13]. Where |Vth| is the threshold voltage for the inverter, KP & KN are the transconductance parameters for PMOS & NMOS, and Vthp & Vthn are the corresponding threshold voltages for PMOS & NMOS.

$$\left(\frac{W}{L}\right)_p \approx 5\left(\frac{W}{L}\right)_n \qquad (3)$$

B. Threshold Inverter Quantization Comparator

According to the input signal, the TIQ comparator in this architecture chooses the reference voltage range for the control circuit's (N-1) bit flash ADC. The control side delay reduction is the TIQ comparator's main goal. It employs two CMOS inverters in cascade as a comparator in order to achieve quick speed and minimal power consumption. The inverter's threshold voltage is calculated using the formula Vth = Vin = Vout. Vin = Vout is expected to cause both transistors to operate in saturation mode, hence the Vth can be computed as "(4)" [13].

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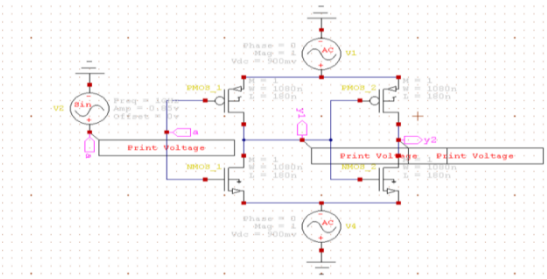

Fig. 5. TIQ Comparator

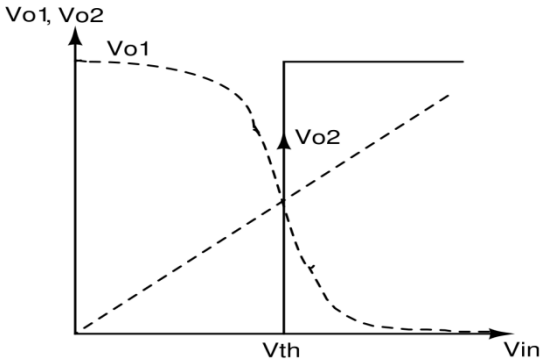

Fig. 6. VTC Curve

$$V_{th} = \frac{r(V_{ref}+V_{tp})+V_{tn}-V_{ref}}{1+r} \qquad (4)$$

$$r = \sqrt{\frac{K_p}{K_n}} = \sqrt{\frac{\mu_n Co_x \left(\frac{W}{L}\right)_p}{\mu_p Co_x \left(\frac{W}{L}\right)_n}} \qquad (5)$$

The hole and electron mobility as well as the transfer characteristics (VTC) are shown in "Fig. 6," which also represents the PMOS and NMOS threshold voltages as Vtp and Vtn, respectively.

Depending on the W/L ratio of PMOS and NMOS, Vth determines the analog input quantization level in the first stage of the inverter. Gain is increased and an unequal propagation delay is prevented using an inverter's second stage.With the help of "(4)" and "(5)," it is possible to represent the width and length ratio of PMOS and NMOS as shown in "(6)."

$$\left(\frac{W}{L}\right)_p \approx 6\left(\frac{W}{L}\right)_n \qquad (6)$$

C. CMOS ROM Priority Encoder

A circuit called a priority encoder reduces a large number of outputs produced by many binary inputs provided by many comparators. The binary representation of the initial number appears as the output. The input with the highest priority will be used when multiple inputs are submitted simultaneously. The main parts of the encoder are thermometer code to 1 out of N code converter [14] and 1 out of N code to a similar binary code converter. To implement the converter from thermometer code to one out of N code, NAND and NOT logic gates are employed. Another code converter that transforms a 1 out of N code into its binary counterpart uses PMOS and NMOS transistors with one end connected to VDD. The output of the comparators is created and fed into the NAND logic section. The thermometer's coding will be changed so that every other bit is high and one bit is low. This code is fed into a CMOS ROM binary encoder. The bit line is drawn to VDD when the PMOS is at logic low and pushed to ground when the NMOS is at logic high.This encoder functions much more quickly due to the reduced propagation latency brought on by the parallel design. In "Fig. 3," a schematic representation of a CMOS ROM priority encoder for building a 6-bits enhanced flash ADC is shown.

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The ratio of the width and length of the NMOS and PMOS driver transistors is found in "(7)" in the CMOS ROM priority encoder. Similar to how "(8)" shows how the width and length of the NAND gate relate to one another.

$$\left(\frac{W}{L}\right)_p = 3\left(\frac{W}{L}\right)_n \quad (7)$$

$$\left(\frac{W}{L}\right)_p = 1.255\left(\frac{W}{L}\right)_n \quad (8)$$

D. Comparator

The circuit diagram for a two-stage open-loop CMOS comparator is shown in "Fig. 7". A comparator is a device with a binary output. Practically speaking, the comparator qualities aren't ideal because of an input offset voltage (VOS). The output is therefore unchanged until the input difference approaches VOS.

$$V_o = \begin{cases} V_{OH} & V_{in+} - V_{in-} > V_{IH} \\ A_V(V_{in+} - Vin_{in-}) - A_V V_{OS} & V_{IL} < V_{in+} - V_{in-} < V_{IH} \\ V_{OL} & V_{un+} - V_{in-} < V_{IL} \end{cases}$$

The input offset can be lessened or ignored with the right layout. The comparator output shouldn't change when the input step is small enough, resulting in a linear transient response. If the input step size is large enough, the comparator's output will change since there isn't enough current to charge or discharge the load capacitance. When the input signal fluctuates by 10 mV (from -5 mV to 5 mV), the output will fluctuate by 1.8 V. (from 0 to 1.8 V). In this case, the comparator gain is greater than 10,000 (=10 V/10 mV).

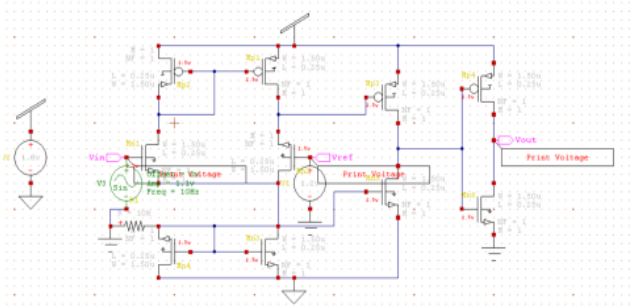

Fig. 7. CMOS Two Stage Open Loop Comparator

E. Implementation of the proposed 6 bit Flash ADC

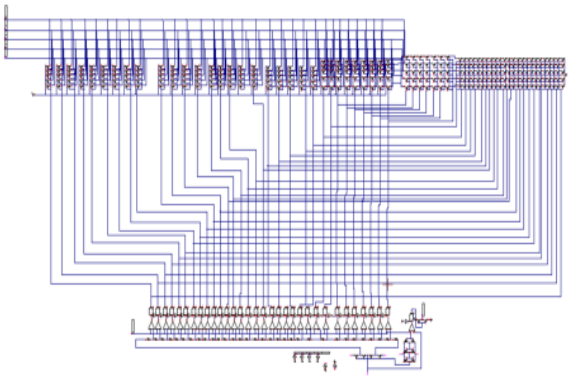

Fig. 8. Implementation of Proposed 6-bit Flash ADC

The suggested 6 bit Flash ADC's implementation is shown in Fig. 9. The comparator's input (Vref) is made up of a 32-resistor resistor ladder network. Here, the control circuit provides an automatically switched reference voltage to the input signal, which is based on a resistive divider network. The 6 bit Flash ADC includes 32 Comparators that compare the two inputs, +Vref or -Vref and Vin. The TIQ comparator establishes the reference voltage range for (N-1) bit flash ADC.The thermometer code is the output of the comparators. In order to enable a single input that be fed into it, the ROM encoder will convert into a digital output and produce a digital output based on input precedence.

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V. SIMULATION RESULTS

A two-stage open-loop comparator with 180 nm CMOS technology is used to design and implement the suggested ADC architecture. The Tanner tool, which is sold commercially, is used to run the simulations. Using transient analysis, the performance of the developed control circuit is examined. With a voltage range of -1.8 V to 1.8 V, the control input is regarded in this case as a clock pulse.The control circuit verifies that, as illustrated in "Fig. 9," the midpoint voltage VK (0 V) is the point at which the reference voltages +Vref (+1.8 V) and Vref (-1.8V) transition. In response to the input signal, the comparator generates the proper control input. The results of the control circuit are shown in "Fig. 9". The output node V1 is charged up to +1.8 V and the output node V2 reaches up to 0 V when the control input is at logic low (-1.8 V). Similar to this, the output nodes V1 and V2 are discharged up to 0 V and -1.8 V, respectively, if the control input is at logic high. Using simulations, it has been determined that the control circuit uses about 3.16µW.

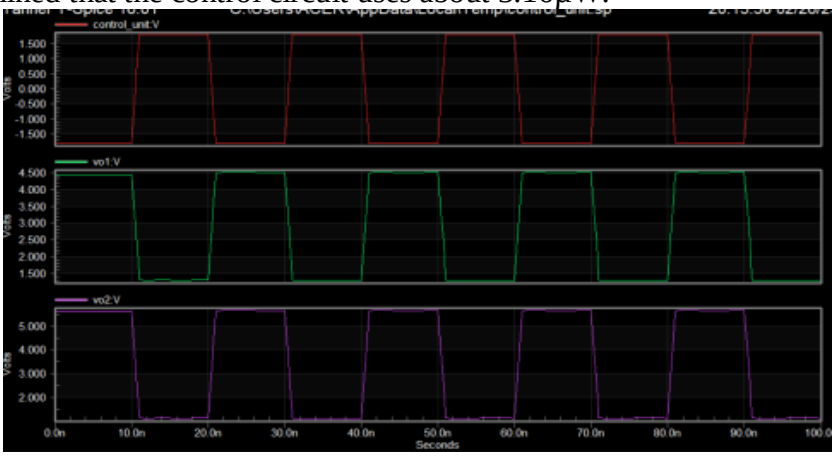

Fig. 9. Results of Control Circuit

The operation of a two-stage comparator is examined through simulation. The VDD and VSS are fixed at 1.8 V and -1.8 V, respectively. The reference signal's amplitude is set at 900mV in. The input signal is assumed to be a sine wave with a frequency of 1 GHz. The input signal's frequency will have an impact on the offset of the comparator. The comparator output is high when the input signal exceeds the reference signal and low otherwise. The comparator circuit consumes roughly 35.92µW of power, it should be mentioned.

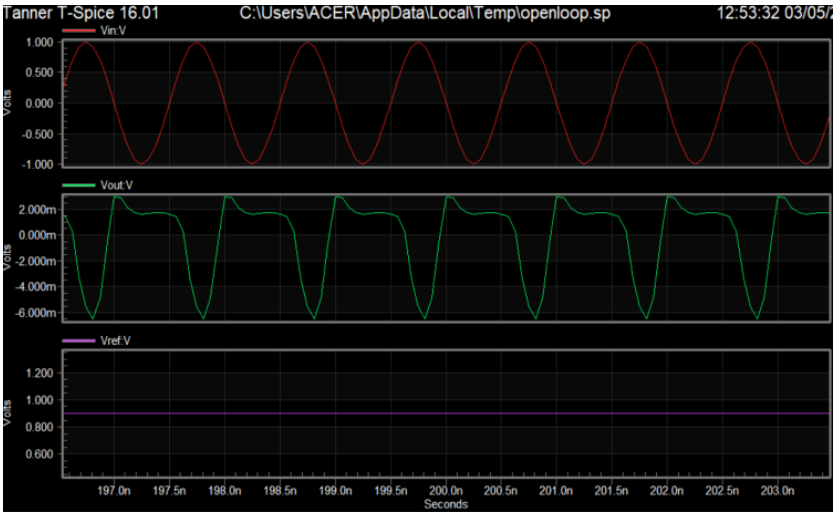

Fig. 10. Results of CMOS Comparator

Performance of the created TIQ comparator is examined. The width and length ratios of nMOS and pMOS are computed through "(6)" while accounting for the reference voltage (threshold voltage) of 900 mV. If the input signal voltage is greater than the reference signal voltage, the comparator's output is low, as shown in "Fig. 11". This TIQ comparator consumes 891.025 pW of power.

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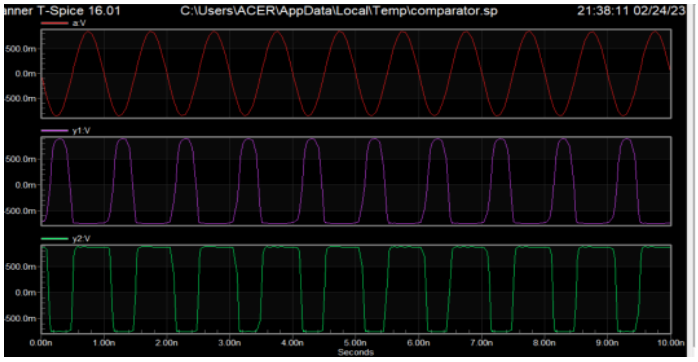

Fig. 11. Results of TIQ Comparator

The performance of the suggested 6-bit flash ADC design is then assessed using the transient analysis, as illustrated in "Fig. 12". Digital codes between 0 and 63 are generated in accordance with the output. The outcomes show that the flash ADC is performing according to plan. The effectiveness of the flash ADCs is contrasted in "TABLE I." Less transistors are required when comparing the proposed flash ADC to the current flash ADC. With this architecture, performance is improved without demanding extra power or space.

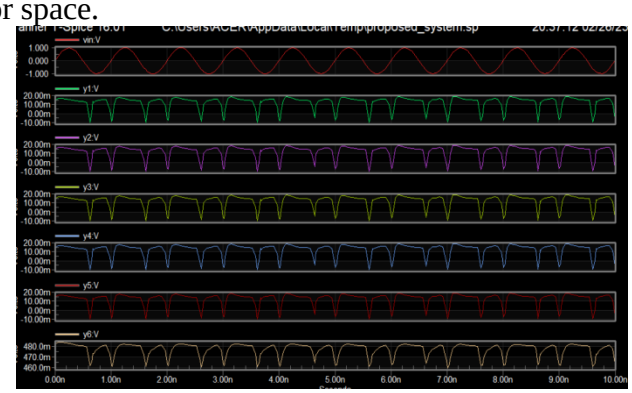

Fig. 12. Transient Analysis for 6-bit Proposed Flash ADC

TABLE I. PERFORMANCE OF PROPOSED METHOD

Architecture	Power consumption	Delay	Transistor Count
Control Circuit	3.16µW	5.001ns	4
NOT-NAND Logic	161.02pW	68.67ps	6
Two Stage Comparator	35.92µW	81.58ns	10
TIQ Comparator	891pW	254ps	6
5-Bit CMOS ROM	620.49pW	49.8ns	346
6-Bit Existing Architecture	1.15mW	1.445µs	1392

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6-Bit Proposed Architecture	595.78µW	1.465µs	658

VI. CONCLUSION

The proposed 6 bit flash ADC and related sub-blocks are designed using the 180 nm CMOS technology. The sub-blocks of ADC like resistor ladder network, comparator, control circuit and TIQ comparator are implemented and simulated. The proposed architecture requires only 32 Comparators so it is an advantage compared to conventional ADC, as it greatly reduces the area with a less number of transistors. The proposed design uses 658 CMOS transistors , where as in the conventional flash ADC, 1392 CMOS transistors were used. The proposed 6 bit flash ADC operates at 1GHz input signal frequency and dissipates power of 595.78 µW with a maximum delay of 1.465 µs.

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