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Design of FIR Filter Based on HDL Coder

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Abstract
HDL Coder is a common Verilog code generation tool. An FIR filter is used with basic structure, word length and coefficients is built, and Verilog code is generated by using HDL Coder tool. The result shows that HDL Coder has advantages in consumption in logic elements and pin consumption. Majorly advantange in logical elements consumption. So, power consumption is reduced. Due to this area will be reduced power dissipation also reduced.

Introduction
With the rapid development of VLSI, digital signal gradually replaces analog signal in more and more application fields, and shows strong advantages [1]. In the field of digital circuits, most of them need software programming to assist hardware design. In most of the fields involved in the digital integrated circuit industry, VHDL/Verilog code is needed to describe system functions, while handwritten VHDL/Verilog code is a very time-consuming and laborious thing.
HDL Coder is a toolbox which can transform MATLAB code/Simulink model into VHDL/Verilog code introduced by MathWorks [3]. It allows engineers to use MATLAB to realize FPGA and ASIC design, greatly improving the working efficiency of system engineers and speeding up the process of FPGA system level design and development.
In this paper, we focus on the use of the above two code generation tools. Taking 16-tap FIR low-pass filter as an example, we use MathWorks's HDL Coder to generate Verilog code, and then complete the simulation waveform in Modelsim. According to the technical report provided by Quartus II, the resource consumption is compared to identify the advantages and disadvantages of the tool.

Theories of FIR filter
The purpose of digital filter is to process the sampled data by mathematical operation. The system function of an M-tap FIR filter system is shown as [4]:

$$H(z)=\sum_{K=0}^{M} bk\, z^{-k} \quad (1)$$

Where *M* is the number of delay sections, also known as the taps of FIR filter. The basic FIR filter can be expressed as follows.

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$$y(n)=\sum_{i=0}^{L-1} x(n-i)\, h(i) \quad (2)$$

Where *x(n-i)* is the input sampling sequence, *h (i*) is the filter coefficient, *L* is the length of filter coefficient, *y (n*) represents the filter output sequence. Convolution can also be used to express the relationship between output sequence *y(n*) and *x(n*), *h (n*) as:

$y\,(n) = x\,(n)*h\,(n)$ (3)

Figure 1 shows a typical direct I-type 3-tap FIR filter whose output sequence *y*(n) satisfies the following equation:

$y\,(n) = h(0)\,x(n) + h(1)\,x\,(n-1) + h\,(2)x(n-2) + h(3)\,x\,(n-3)$ (4)

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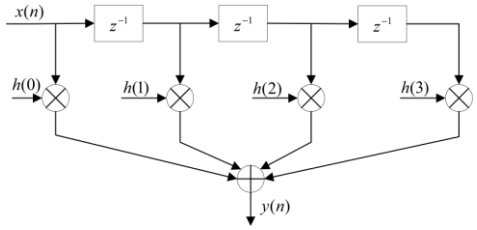

Figure 1. The structure of 3-tap FIR filter

As shown in Figure 1, there are four multiplication units, three delay periods and one four-input adder in this 3-tap FIR filter. If the conventional HDL is used, the instructions can only be executed serially, so it is impossible to complete the whole process in the same instruction cycle. The advantage of using FPGA is that it can adopt parallel structure, and the output of FIR filter can be obtained in one clock cycle.

2.1HDL Coder

HDL Coder is a tool developed by MathWorks. Its main function is to convert MATLAB code/Simulink model into VHDL/Verilog code. In order to complete the comparison between DSP Builder and HDL Coder, we use HDL Coder to design an FIR filter when the structure of filter, word length and filter coefficients are the same. MATLAB code and Simulink model are equivalent and Simulink model is more intuitive to use. Here we use Simulink model to design FIR filter. The Simulink model of a 16-tap FIR lowpass filter with the same index is shown in Figure 7, and the simulation result in MATLAB is shown in Figure 8.

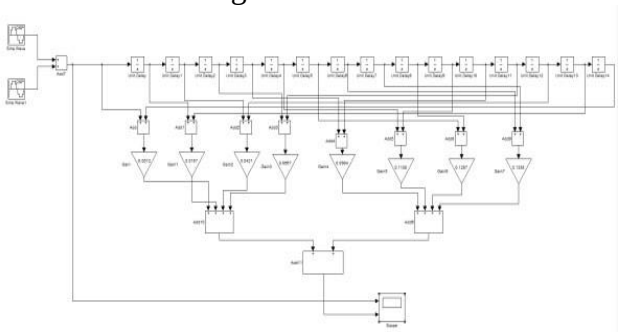

Figure 7. Simulink model of 16-tap FIR filter

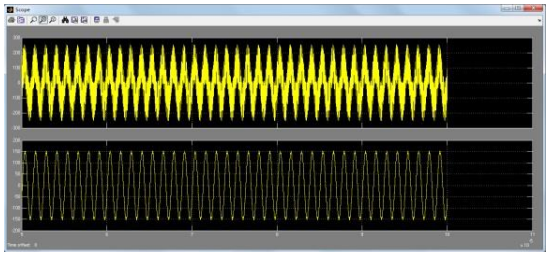

Figure 8. Simulation result of 16-tap FIR low pass filter in MATLAB

Using HDL Coder to generate Verilog code is mainly divided into three parts: generating fixed-point function; generating Verilog file; generating testbench file. We simulate the generated Verilog file in Modelsim, and the result is shown in Figure 9.

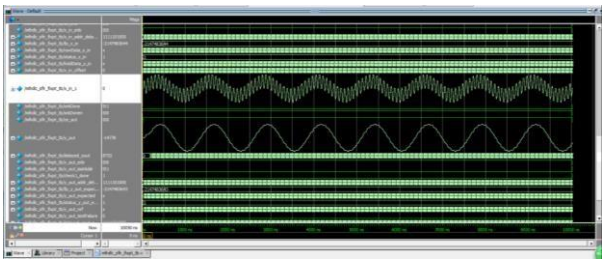

Figure 9. Simulation result of 16-tap FIR low pass filter in Modelsim

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Discussion

We select several FPGA devices and use the Verilog code generated by HDL Coder to synthesize in Quartus II. Then the consumption of total logic elements and total pins is showed. The results are shown in Table 1.

Table 1. Results on five devices

Device	Technology	Logic elements	Pins
EP1S10 F484C5	HDL Coder	212/10570 (2%)	102/336 (30%)
EP2S15 F484C3	HDL Coder	112/12480 (1%)	102/343 (30%)
EP4CE 6F17C6	HDL Coder	156/6272 (2%)	102/180 (57%)
EP2C5 F256C6	HDL Coder	156/4608 (3%)	102/158 (65%)

For total logic elements. EP1S10F484C5 has more logical elements than remaining FPGA devices. Therefore, Series F484C3 series logical elements are 1 % and remaining FPGA series have more logical elements consumption. Coming to pin consumption Series F484C5 and F484C3 has 30 % than remaining series. Remaining series have more pin consumption. So, F484C5 has advantages in pin consumption.

1. Summary

In this paper, we take the design of FIR filter as an example to compare the resource consumption of Verilog code generated by HDL Coder in FPGA. The results show that HDL Coder has advantages to show the pin consumption and the consumption of logic elements.

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