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Different Leakage Power Reduction Techniques Comparison in CMOS VLSI Design

[1]Ms. S. Bhavani, [2]R. Rasi, [3]S. Hibza, [4]M. Samatha [5]B. Veerendra Reddy, [6]K. Vinay
[1]*Assistant Professor, Department of ECE, AITS, Tirupati, A.P.*
[2,3,4,5,6]*B. Tech Student ,Department of ECE, AITS, Tirupati, A.P.*

Abstract
Gadgets consuming less power have risen as a well-known subject in the cutting-edge electronics industry. Decrease in consumption of power makes a device increasingly dependable and productive. As a result, CMOS innovation turned out to be most popular for low power utilization gadgets. Cutback on the voltage supply decreases the dynamic power loss quadratically and the leakage power linearly. Weak inversion current due to leakage is a prime candidate for standing power utilization. Since the feature sizes continue to reduce it has caused an exponential rise in weak inversion current due to leakage thanks to the reduction of sub-threshold voltage. As stated in the previous works, leakage power dissipation sooner or later may tower above the total power consumption as the size of technological features reduce to nano-meter scheme in submicron technologies. This paper is aimed to bring a thorough analysis and comparison of various leakage power reduction techniques used.

Keywords— *leakage current sub-threshold voltage, deep submicron, power gating, CMOS, LECTOR, power dissipation, Propagation Delay.*

INTRODUCTION

With the ongoing developments in VLSI innovation, transistors' requests in Integrated Circuits are yet developing, which requests costly cooling and bundling advancements. Subsequently, because of this, the supplied voltages are downsized for diminishing the power dissipation. Be that as it may, scaling of supply voltage has brought about an exponential increase in sub-threshold leakage current, causing static (spillage) power dissemination. In the present life, the primary spotlight is on low power gadgets on account of development in mobile devices; and however, even before the introduction of mobile devices, power dispersal was an endless issue. Higher power utilization prompts lower execution and reliable quality of the circuit. There are numerous strategies to lessen the leakage power. Static power constitutes about half of the all-out power utilization in the present high-performance chips. As per the need, a decrease of leakage power is the way into a low force VLSI plan.

$$Pleak = Ileak*VDD$$

Where,

I leak - When the transistor is OFF, the Spillage current which streams in it.
VDD – Voltage supplied
Pleak – Power leaked

The leakage current is directly proportional to the leakage power. Therefore Ileak must be reduced to get reduced leakage power Pleak. The leakage power commands the dynamic power, especially in crucial VLSI circuits and what's more in the circuits that leftover parts in the inertly mode for an extended time, for example, cell power. In real life, every application draws out the battery life anyway. With a developing pattern towards portable computing and remote communication, power dissemination has turned out to be one of the most basic components. In this way, the primary spotlight is on the decrease of leakage power.

As the technology pattern took another stage, leakage power expanded exponentially with more transistors' reconciliation on the substrate. The leakage power is said to be that static force scattered

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when there is no useful outcome from the current or when the circuit is out of gear state. When gate voltage (Vg) in the transistor is lower than the Vth, i.e., threshold voltage, the transistor can't be totally turned off, which prompts little current flow called **leakage current**.

POWER DISSIPATION FACTORS IN CMOS

A. Leakage Power

Leakage power is the power consumed by the transistor in off state due to reverse bias current. It is usually assumed that when off, transistors are not supposed to pull any current but even in this off state a small amount is drawn due to reverse bias current in the diffusions, as well as weak inversion current due to the inversion charges, all of this is together termed as leakage current and the power dissipated as a result of this is leakage power

B. Junction Leakage

Between the diffusion region and the substrate, certain diodes are formed which are accountable for power consumption through the way of reverse bias current. Because of electron hole pair generation in the reverse bias junction depletion region and a drift near the depletion region, junction leakage is produced. As it is observed in many MOSFETs, the n and p regions are heavily doped so junction leakage will also be there.

CAUSES OF LEAKAGE POWER DISSIPATION

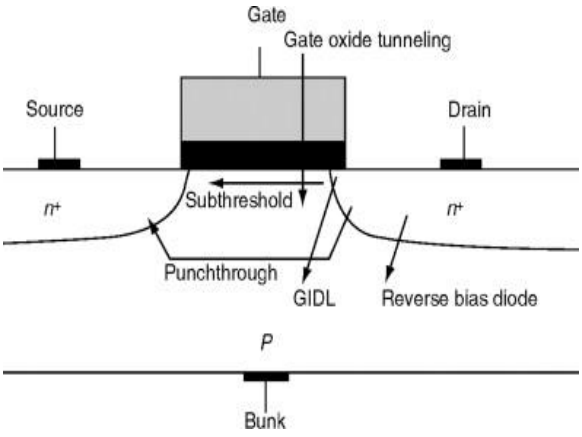

Fig 1: Types of Leakages in CMOS Circuit

1. Leakage due to junction current

As it was discussed above certain type of junctions or diodes are formed in the reverse biased conditions which are responsible for power consumption in the circuit. The rate of infusion of minority carriers sees a rise with a rise in temperature which in turn gives rise to an increase in leakage current.

2. Weak inversion current

When the gate to source voltage is less than that of threshold (off state), this causes a leakage current to travel in a path from drain to source, this is termed as weak inversion/weak inversion current. When the voltage at the gate is just below that of threshold, the current is at its peak value. With the modern day technology and the industry scaling down the voltage rigorously, it is turning out to be an important contributor in leakage power.

3. GIDL

GIDL or Gate Induced Drain Leakage is an event which occurs when the gate overlaps the drain by means of applying high voltage to the drain and keeping the gate grounded [3]. It causes tunnel based leakage current in the region where the overlap occurred. This current's increase is directly

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proportional to that of the drain voltage and it is key contributor in causing extreme heat and an increase in leakage power.

4. Oxide leakage tunnelling

In the contemporary times the dimensions of the transistors being used are decreasing every year. As a result the thickness of the gate oxide is also reducing in order to deliver better performance. However in order to go for high performance this thinning of the oxide layer has caused leakage current to travel between the substrate and the gate through the oxide.

TECHNIQUES FOR LEAKAGE POWER REDUCTION

DTMOS

DTMOS technique is a principally used technique in digital circuits during which MOSFET's gate and body are tied together [4]. As it has very great advantage of MOSFET as it reduces the current due to leakage and provides high threshold voltage during off state and shows low threshold voltage during on state to increase the current driving capabilities of the circuit. Whenever the transistor is on, the threshold voltage and propagation start decreasing and this causes the current to increase as shown in Fig. 4. Similarly when transistor is OFF, its threshold voltage increases, current due to leakage reduces and power consumption also minimizes. DTMOS provides less delay with increased speed.

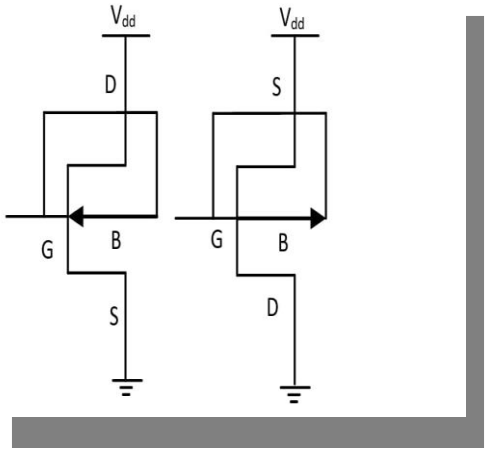

Fig 2: DTMOS Structure

DTMOS devices are efficient because they function as dual threshold logic gates. It is an excellent Scheme to provide less delay with increased to traditional body biasing in the sub-threshold region.

MTCMOS

MTCMOS is a technique which makes use of multiple threshold voltages in order for optimization of delay and power by making use of high threshold sleep transistors for low leakage currents and low threshold transistors(cells) for ensuring high performance of logic gates. In this technique high threshold voltage transistor are used to isolate the low threshold voltage transistor from supply and ground during standby mode. However by including extra transistor, MTCMOS circuit faces performance penalty compared to CMOS circuits, if the transistor are not sized properly.

The high threshold voltage transistor are turned off during standby (sleep mode), this result very low sub threshold passes from Vcc to ground. MTCMOS includes high Vt transistor to gate power and ground of a low Vt logic blocks as shown in figure 3. When the high Vt transistor are off resulting in a very low sub threshold leakage current. When the high Vt transistor are turned on, low Vt are connected to virtual ground and Vdd.

The delay for both CMOS and MTCOMS techniques was the same. MTCMOS gave lower average power consumption but a lower power delay product in comparison to the conventional CMOS as well.

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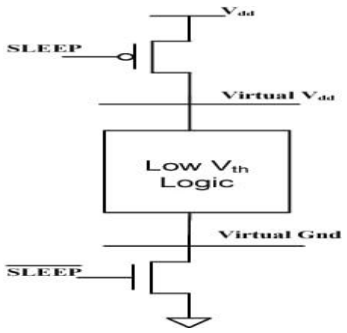

Fig 3: MTCMOS Structure

LECTOR

In this technique two leakage control transistors are used to control leakage current. These two leakage control transistors are introduced within the logic circuit so that one of them is close to its cut-off as shown in Fig. 7. This will increase the path resistance from source to ground, leading to vital decrement of current due to leakages. This works effectively in each active mode conjointly as at intervals the standby mode. The LCT transistors are connected in such a manner so that one of the LCT transistors will be in off state for any input signal. Further, the gate of p-channel and n-channel MOSFET is connected to the drain terminal of n-channel and p-channel MOSFET respectively. This technique gives an advantage of reducing the leakage current in the path from VDD to ground. The connection between pull-up and pull-down is connected with leakage control transistors. By breaking the path between PMOS and NMOS reduces the leakage current.

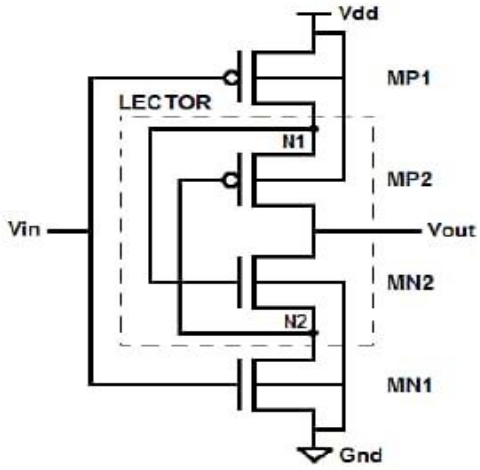

Fig 4: LECTOR Structure

ONOFIC

The On/Off logic (ONOFIC) approach reduces the leakage current and power with single threshold voltage level approach. This technique efficiently reduces the leakage current in both active and standby mode of logic circuit. Same as LECTOR technique the ONOFIC approach also introduces an extra logic between pull-up and pulldown networks for leakage reduction. This additional introduced circuit is called On/Off logic (ONOFIC) circuit. ONOFIC approach contains one PMOS and one NMOS transistor. Due to maintaining either on or off condition for any output logic level this technique is known as ONOFIC. The connection of ONOFIC is shown in figure.5. This technique provides the maximum resistance to the ONOFIC block when it is in off state and minimum resistance when it is in on state. This logic directly affects the power dissipation and propagation delay of the logic circuit.

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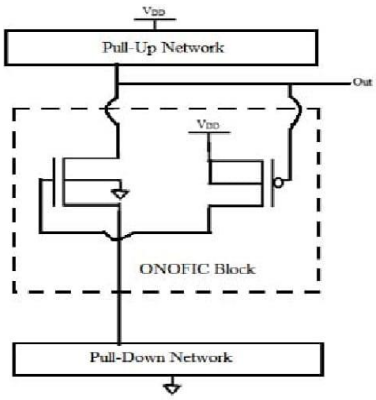

Fig 5: ONOFIC Structure

In ONOFIC block, the drain of PMOS transistor is connected to the gate of NMOS transistor and the output is connected to the gate of PMOS transistor. The drain of the pull-down network is connected to the source of NMOS transistor and PMOS source terminal is connected to VDD of the circuit. The NMOS transistor drain is connected to the output of the circuit and the substrate of NMOS transistor is connected to the ground while the substrate of PMOS transistor is connected to the VDD. The main concept of this technique is property of On/Off. The both ONOFIC transistors are in linear region when ONOFIC logic is in on condition while ONOFIC logic is in off state both the transistors are in cut-off mode. The good conducting path is obtained by turning on the ONOFIC block and it acts as a good resistance to control the leakage current when it is in off state.

ONOFIC had better delay and power delay product than LECTOR and CMOS but a higher power dissipation as well. LECTOR had the lowest power dissipation.

CIRCUITS FOR PROPOSED TECHNIQUES

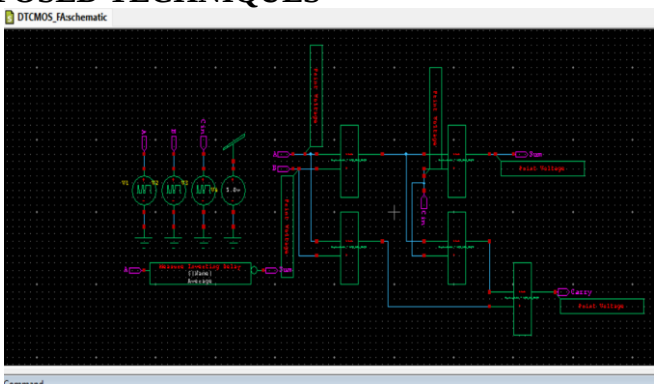

Fig 6: Proposed DTMOS full adder circuit

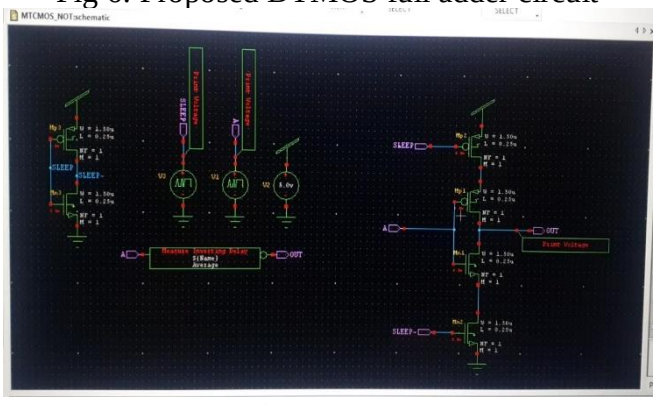

Fig 7: NOT design using MTCMOS

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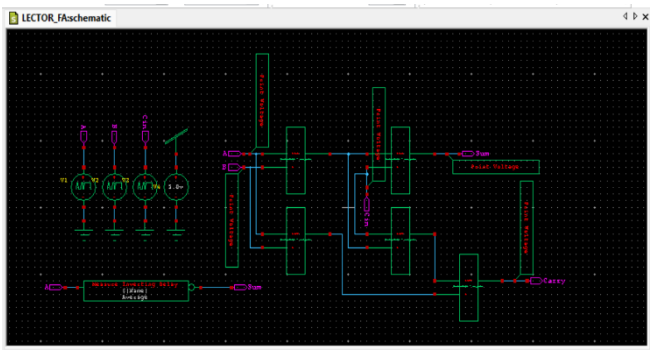

Fig 8: proposed LECTOR full adder circuit

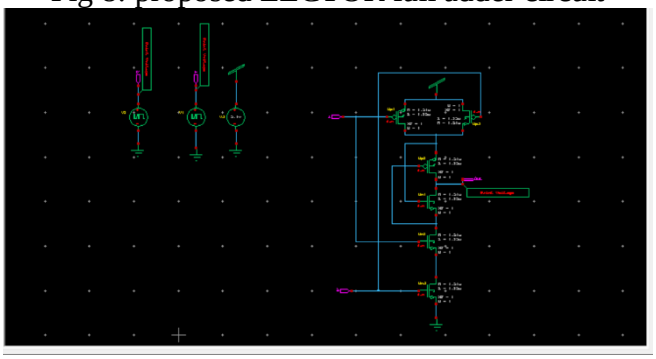

Fig 9: NAND design using ONOFIC

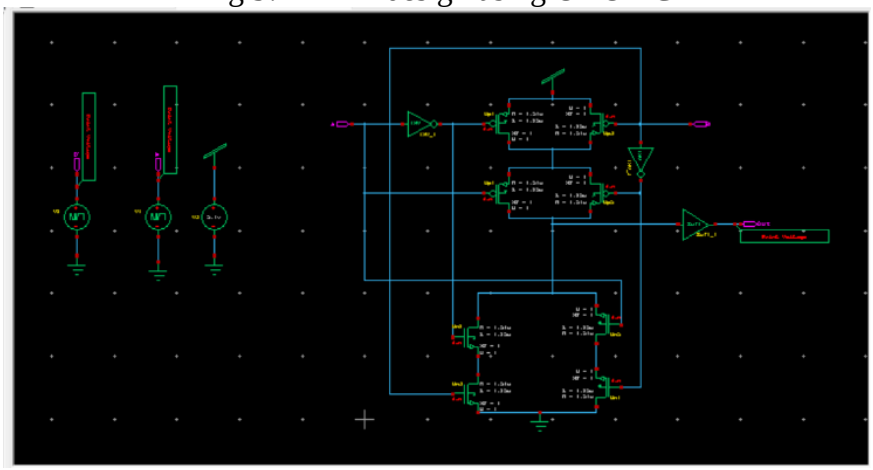

Fig 10: XNOR design using ONOFI

RESULT AND SIMULATIONS

RESULT

TABLE: Comparison based on Leakage Reduction Techniques □□□□□

Parameters / Techniques	AREA (No. of MOSFETs)	Power Dissipation(W)	Propagation Delay(sec)	Performance
CMOS	42	0.8223mw	0.71 seconds	Good
DTMOS	42	0.9518mw	1.08 seconds	Good
MTCMOS	52	0.6731mw	0.69 seconds	Good
LECTOR	66	0.2491mw	0.76 seconds	Good
ONOFIC	16	0.5494mw	0.35 seconds	Good

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SIMULATIONS

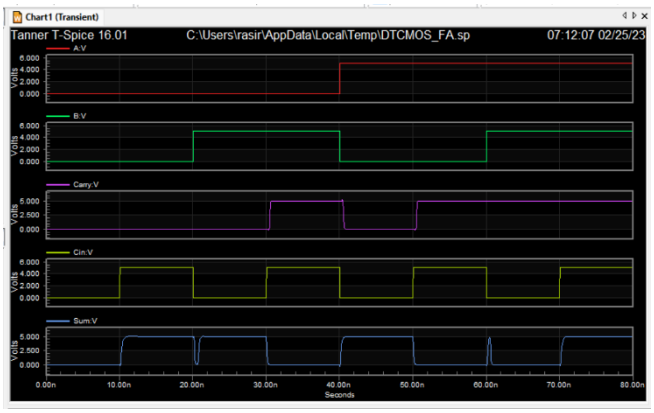

Fig 11: Input-Output waveform of proposed DTMOS circuit

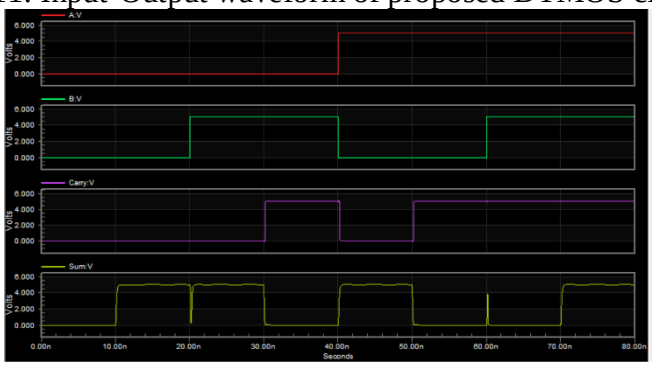

Fig 12: Input-Output waveforms of proposed MTCMOS circuit

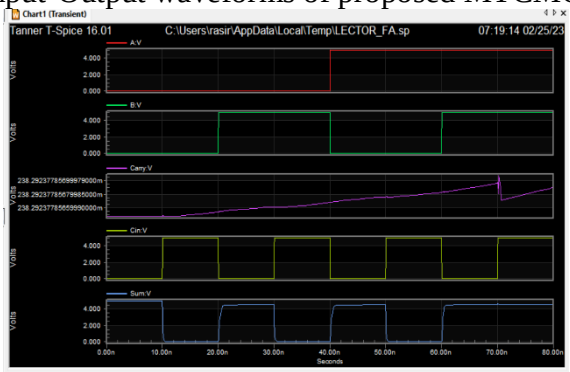

Fig 13: Input-Output waveform of proposed LECTOR circuit

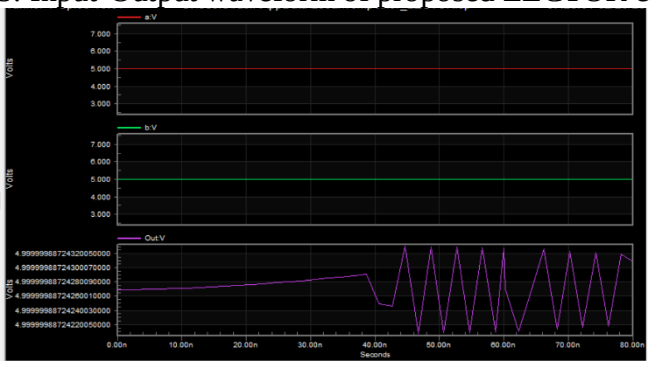

Fig 14: Input-Output waveform of proposed ONOFIC circuit

CONCLUSION

Scaling down of the technology has led an increase in current due to leakage. In this day and age leakage power has turned out to be more prevailing in comparison to Dynamic power but, Dynamic Power consumption thanks to glitches can't be neglected. In this paper our main aim was to give a comprehensive analysis and comparison and performing statistics of the numerous power reduction

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techniques both new ones like ONOFIC and ones which have been used in past works. We also covered the trends of power dissipation which we have seen over the decades and discussed the various key contributors of leakage power dissipation. All the modern-day research and analysis regarding the leakage power reduction techniques will prove to be helpful for someone looking to use all or some of them in an application. It can be observed that all the prominent terms like dynamic power, leakage power, propagation delay and power delay product all have a strong interrelation and may affect the other in a direct or indirect way. However, it cannot be denied that improvement of one parameter majority of the times in trading off the performance of the other parameters.

In CMOS circuits, leakage power has become a more dominating component of total power consumption in battery oriented applications. Our proposed full adder techniques gives low power dissipation when compared to other circuits. Here in this project, the problem of power dissipation is reduced for different VLSI CMOS circuits. We simulated all circuits by using Tanner EDA. It is helpful in saving power by reducing leakage power. Hence, It was observed that when it came to power dissipation LECTOR performs better than ONOFIC but in matter of propagation delay ONOFIC is better than LECTOR technique.

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