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Implementation of Error Detection andCorrection Codes for Space Engineering Applications using VLSI

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Abstract
Because of technological scaling, on-chip memories in a die experience bit errors as a result of single events or multiple cell disruptions caused by environmental factors like cosmic radiation, alpha and neutron particles, or the space environment's maximum temperature. This results in data corruption. The damaged data over a communication channel is identified and corrected by error detection and correction techniques (ECC). It is suggested in this research to weaken radiation-induced MCUs in memory for space applications by using an enhanced error correction 2-dimensional coding based on the divide-symbol. The XOR operation was used to assess the diagonal bits, parity bits, and check bits for data encoding. The encoded bits and the recalculated encoded bits were again XOR ed in order to extract the data. Following analysis, there is a procedure of verification, selection, and correction.Xilinx Vivado was used to simulate and synthesise the suggested design, which was then implemented in Verilog HDL. As compared to well-known existing approaches, this encoding-decoding procedure uses less power, takes up less space, and has shorter latency.
Keywords— *Error Correction Code, Multiple Cell Upsets, Encoder, Parity, Decoder, Memory*

I. INTRODUCTION

Electronic circuits, especially memory susceptible to soft mistakes, perform poorly in space due to high temperatures. Neutron or alpha particles from the earth's atmosphere disrupt memory cells [1]. Increasing the critical charge at the state nodes or using well and substrate approaches are two ways to mitigate these mistakes (process related techniques). Another method is to use error correction codes (ECCs) on memories, which can help to rectify some faults [2]. To handle independent faults, single error correction (SEC) codes are typically used on each memory. Accuracy is increased through SEC scrubbing. It periodically examines memory and fixes minor mistakes so that they don't build up.When two or more bits of the same memory are affected in multiple cell upsets (MCUs), this is ineffective.

The interleaving approach is suggested [4] as a means of overcoming multiple cell disruptions in memories. Many research have been conducted using this method to treat various cell disturbances (MCUs). However, the complexity of the system design is increased by the proposed interleaving mechanism, which also affects the amount of space and power used. ECCs are employed in the event of numerous cell disturbances (MCUs). This necessitates the use of more parity bits, longer decoding times, and more sophisticated circuitry for both encoding and decoding. Several ECCs concentrated on reducing area, latency, and power.

For the purpose of reducing multiple bit upsets in memories caused by radiation exposure, Zhu et al. [5] suggest a new error correction code. In addition to identifying and fixing neighbouring double bit errors, this also reduces errors for double bit faults that are not contiguous. The testing findings show that it is more effective than other ECC codes already in use and decreases hardware redundancy by 40%. High reliability memory system design is achieved by this method's reduction of errors for non-adjacent DBE by 12% in comparison to the traditional SEC-DED-DAEC codes.

With the (24, 12) extended Golay code, Pedro et al. [6] have developed an effective single and double adjacent error correcting parallel decoder. In this parallel decoder, the implementation of the first bit is done using a 12 bit OR gate, and the rest is done using a 24 bit OR gate. Synopsis design compiler

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synthesised twice using HDL and the mapping of TSMC 65 nm technology to cut down on area and latency.

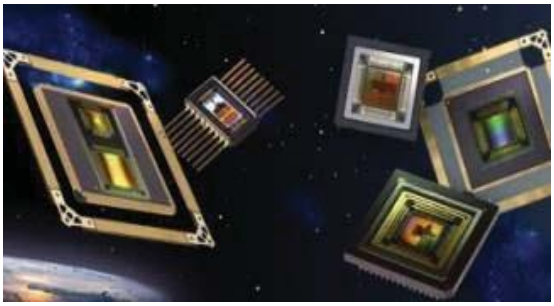

Fig. 1 ICs for space applications

In comparison to the current SEC-DAEC decoder, this translates to reductions of about 45% and 11% for area and 28% and 21% for delay. A new decimal matrix coding ECC is employed to boost the memory reliability in [7].Synopsis Design Compiler creates the encoder and decoder on SMIC 0.18 m technology. According to the results of the simulation, this technique's MTTF for hamming, MC, and PDS, respectively, is 452.9%, 154.6%, and 122.6%, and its latency is 73.1%, 69.0%, and 26.2%. The idea to safeguard the memory from data loss using a different set of codes (cyclic-linear block codes) as ECC is presented in [8]. In order to improve the likelihood of error correction and shorten the decoding process, this strategy takes advantage of the localization of MCU defects as well as DS code properties. The simulation results show that this technique is effective in lowering the decoding time as well as the space and power consumption. It is implemented in HDL. For different data word lengths (16, 32, and 64 data bits), Reviregoet al.[9] proposed a novel algorithm to rectify triple adjacent errors (SEC-DAEC-TAEC) and 3-bit burst errors.The parity check matrix's total number of ones has been reduced to reduce decoding time, while its maximum number of ones in its rows has been increased to increase speed.

For space engineering, Andrew et al. [10] presented a turbo system as well as a low-density parity-check code. This turbo system and LPDC codes are frequently employed in the data transfer for the aeroplane applications. In an encoding-decoding fashion, the error-correcting code with minimal power consumption from space has been introduced. The organization of low-density parity-check codes takes the form of a parity check matrix. When the code rate decreases, the parity check matrix grows, making the decoder more difficult. In comparison to the current error correction codes used in deep space applications, the development of turbo codes and LPDC codes increases the system's efficiency and dependability.Turbo codes can also be created on trellises. For each coding sign, there will be one trellis section or information bit. As a result, turbo codes outperform low-density parity-check codes when used sparingly. This iterative decoding of either turbo or LDPC code is more difficult than other decoding techniques.

With the DVB S2 system, a new forward error correction code (FEC Encoder) with BCH code, LPDC code, and QPSK modulation is introduced[11] . The code length of 64800 bits and half of the standard rate LDPC code are taken into consideration for FPGA implementation. Timing requirements are processed at 122 MHz for the design. To increase coding efficiency, pipelining technology is also used into the design. This study proposes a new encoding-decoding algorithm for multiple cell upset error detection and correction (MCUs). The XOR operation was used to analyse the data bits, diagonal bits, parity bits, and check bits for encoding. Additionally, a second XOR operation was carried out between the redundant bits and the recalculated redundant bits in order to recover the original data.

It includes an introduction and a list of related publications. The remainder of the essay is structured as follows. The suggested ECC algorithm and the encoding-decoding process are described in Section II, while the methodology's results and discussions are presented in Section III, and the conclusions and some ideas for future work are presented in Section IV.

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II. ERROR DETECTION AND CORRECTION SCHEME

A novel error-correcting 2-dimensional code (2D-ECC) is suggested to increase memory dependability. As compared to other existing error correction techniques, this algorithm effectively detects and fixes problems. To recover the original data, this executes data region division, redundancy and syndrome computation, verification, and region selection one at a time. The most used operation in cryptography, boolean XOR, is employed to provide parity bits for error checking and fault tolerance. Fig. 2 depicts the block diagram of the suggested ECC approach.

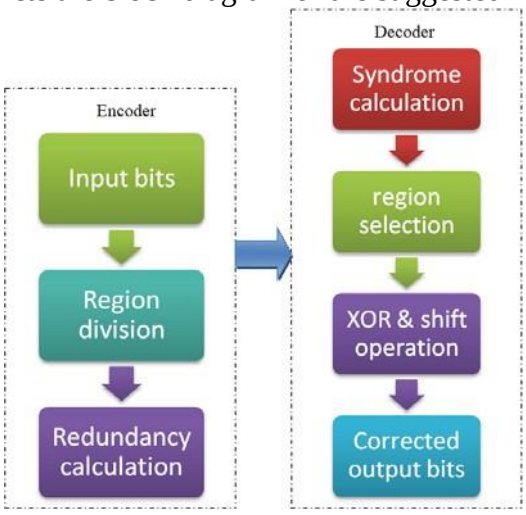

Fig. 2 ECC methodology

This two-dimensional technique executes an encoding-decoding procedure that converts the 16 bit input data into 32 bits during encoding and restores the 16 bit data during the subsequent decoding step.

Proposed algorithm

STEP 1: Read the input 16 bit data(A16-A0).

STEP 2: Divide the input data into 4 groups

X1	**Y1**	**Z1**	**W1**
X2	Y2	Z2	W2
X3	Y3	Z3	W3
X4	Y4	Z4	W4

STEP 3: Analyze diagonal bits, parity bits and check bits using XOR operation

- Diagonal bits (D1, D2, D3, D4) using XOR operation as the 2×2 matrix,

$$D1 = X1 \oplus Y2 \oplus Z1 \oplus W2$$
$$D2 = X2 \oplus Y1 \oplus Z2 \oplus W1$$

- Parity bits (P1, P2, P3, P4) using XOR operation taking the first bits, second bits, third bits and the fourth bits from four groups

$$P1 = X1 \oplus Y1 \oplus Z1 \oplus W1$$
$$P2 = X2 \oplus Y2 \oplus Z2 \oplus W2$$

- Check bits (Cx, Cy, Cz, Cw) using XOR operation bytaking the alternative bits.

$$Cx_{13} = \boldsymbol{X1} \oplus \boldsymbol{X3}$$
$$Cx_{24} = \boldsymbol{X2} \oplus \boldsymbol{X4}$$
$$Cy_{13} = Y1 \oplus Y3$$
$$Cy_{24} = Y2 \oplus Y4$$

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STEP 4: Calculate the syndrome values for diagonal, Parity and check bits by performing XOR Operation between the redundancy data stored and the recalculated redundancy bits(RDi,RCi,RPi).

SDi = Di RDi

SPi = Pi RPi

SCi = Ci RCi

Where i = 1,2,3,4

STEP 5: Check the following conditions to identify the error that to be satisfied

- SDi and SPi bits have at least one value similar to1
- More than one SCi value was similar to 1

STEP 6: Perform region selection and change the erroneousdata to get the corrected output.

Process of encoding:

X_1	X_2	X_3	X_4	D_1
Y_1	Y_2	Y_3	Y_4	D_2
Z_1	Z_2	Z_3	Z_4	D_3
W_1	W_2	W_3	W_4	D_4

P_1	P_2	P_3	P_4
X_1	X_2	X_3	X_4
Y_1	Y_2	Y_3	Y_4
Z_1	Z_2	Z_3	Z_4
W_1	W_2	W_3	W_4

X_1	X_2	X_3	X_4	Cx_{13}	Cx_{24}
Y_1	Y_2	Y_3	Y_4	Cy_{13}	Cy_{24}
Z_1	Z_2	Z_3	Z_4	Cz_{13}	Cz_{24}
W_1	W_2	W_3	W_4	Cw_{13}	Cw_{24}

Fig. 3 Encoding model

The 16 input bits should first be divided into four groups (Xi, Yi, Zi, Wi). The XOR operation is used to determine the diagonal bits (Di), parity bits (Pi), and check bits (Ci). The input 16 bits are changed into 32 bits during encoding (redundancy bits).

Process of decoding:

The encoded data and the recalculated encoded bits have been used to assess the syndrome calculation during decoding (SDi, SPi and SCi). Following that, it is possible to undertake verification, region selection, and rectification.

X_1	X_2	X_3	X_4	X_1	X_2	X_3	X_4	X_1	X_2	X_3	X_4
Y_1	Y_2	Y_3	Y_4	Y_1	Y_2	Y_3	Y_4	Y_1	Y_2	Y_3	Y_4
Z_1	Z_2	Z_3	Z_4	Z_1	Z_2	Z_3	Z_4	Z_1	Z_2	Z_3	Z_4
W_1	W_2	W_3	W_4	W_1	W_2	W_3	W_4	W_1	W_2	W_3	W_4

Region 1 Region 2 Region 3

Fig.4 Different regions of data bits

Regions 1, 2, and 3 should be created from the data bits. To achieve effective outcomes, this is created by separating the data bits into the following columns: 1&2, 3&4, 2&3, and so on.

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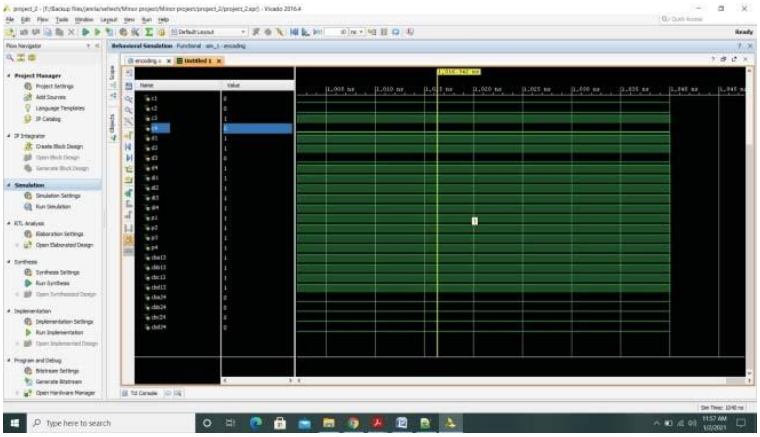
Region	Selection criteria	
Region1	SD1+SD2+SP1+SP2 SD3+SD4+SP3+SP4	>
Region2	SD1+SD2+SP1+SP2 SD3+SD4+SP3+SP4	<
Region3	SD1+SD2+SP1+SP2 SD3+SD4+SP3+SP4	=

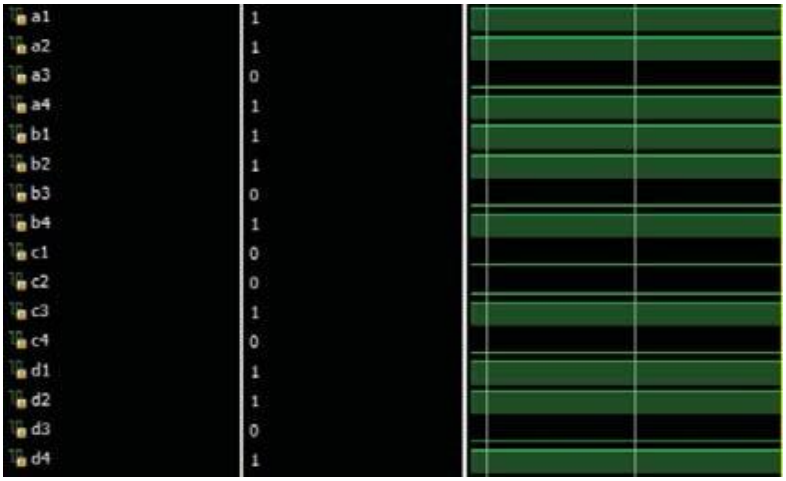
Table 1 Region

The equations in Table 1 were created using SDi and SPi. The error bits are present in regions 1 and 2, which have more syndrome bits equal to 1, and in region 3, where both equations are true. The approach could be utilised extensively in the field of space engineering for bit detection and error correction during data transmission.

III. RESULTS AND DISCUSSION

The suggested 2-dimensional approach is capable of detecting and correcting multi-bit mistakes. It is simulated and generated using Xilinx Vivado 2016.4 in Verilog HDL. The results of the simulation are shown in figures 5 and 6.





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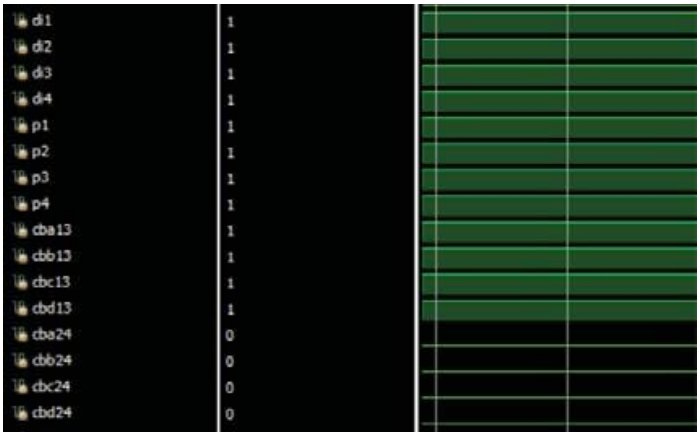
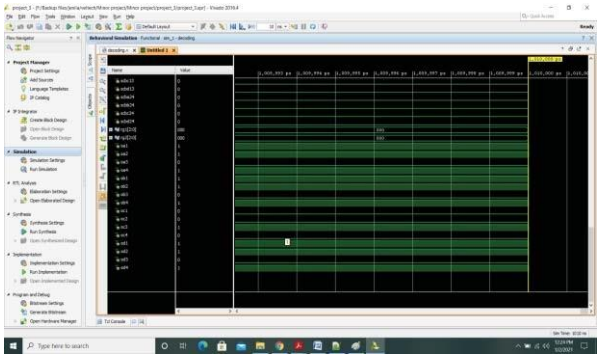
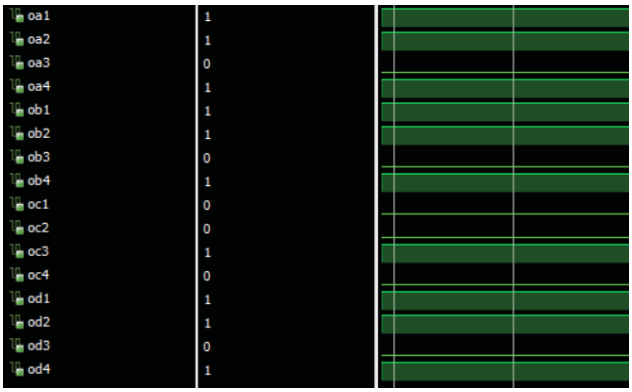


Fig. 5 Proposed encoding output

Decoding is then done to obtain the corrected output 16 bits after the input 16 bits and redundant 16 bits have been stored in memory as 32 bits.





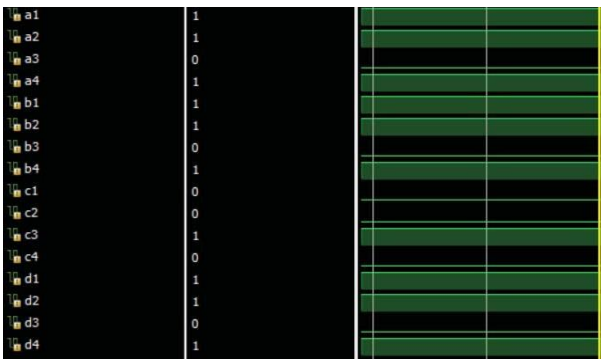


Fig. 6 Proposed decoding output

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The outcomes of the encoding and decoding procedure are shown in Figs. 5 and 6, which show that the output end is able to obtain the identical original data after decoding. In the decoded side, the input data must be recovered without any bit errors. This algorithm has the potential to dramatically do that. The slices, LUTs, and IOBs required
for the design of the encoder and decoder are shown in Table 2.
Also, when compared to other existing techniques, the encoder and decoder circuits' power consumption is extremely low. The comparison parameters for encoder and decoder are shown in Fig. 7.

Parameters	Encoding	Decoding
No of Slices	2	6
LUTs	8	20
Bonded IOB	32	47
Power	0.167W	0.127W

Table 2 Device Utilization Summary

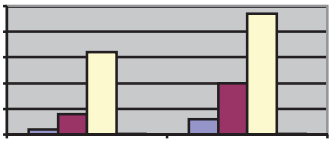

Fig.7 Comparison of Encoder and Decoder

IV. CONCLUSION

In order to lessen data corruption in volatile memories, a novel error correction code (ECC) is suggested in this study. Xilinx Vivado was used to simulate and synthesise the suggested design, which was then implemented in Verilog HDL. Encoding and decoding require 0.167W and 0.127W of electricity, respectively. In comparison to widely used existing technologies, this encoding-decoding procedure uses little power, takes up little space, and has a short delay.This algorithm will also be expanded in order to save space, time, and energy. The decoder area grows in comparison to other approaches since the regions were carefully chosen.Using the advanced region selection criteria further reduces this.

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