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Efficient Approaches to Design Full Adder Using Domino Logic Technique

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ABSTRACT
Static CMOS and Domino CMOS Circuits are significantly used in high performance VLSI system. Designing a circuit with low power, high speed performance is one of the challenging aspects. In modern VLSI systems area efficient devices are utmost popular because most of the devices are becoming portable. This paper proposes One- bit full adder circuit is designed using CMOS based on mirror logic and Domino CMOS also designed based on same logic with LTSPICE at 180nm technology with 1.8V supply. This method provides better power and delay.
Key words: CMOS Full Adder, Domino Logic Full Adder and Mirror Logic.

1. Introduction

In the fast-growing VLSI industry, transistor density is increasing with rapid rate day-by-day .According to Moore's law transistor density will get doubled itself after every eighteen months. As the number of transistor will increase, correspondingly area, delay and power consumption of the device will also increase .So ,a technology is required by which the area can be reduced and increase the performance of the device. From the past few decades CMOS technology [1] is being used for designing the chips in semiconductor Industry ,but as the number of transistor are increasing ,area of the device and delay both are increasing .So it requires to switch to a technology ,which uses lesser area and smaller delay. Hence, the domino logic is used for designing the one-bit full adder and compared the various performance parameter like area, delay, and power consumption in both technology

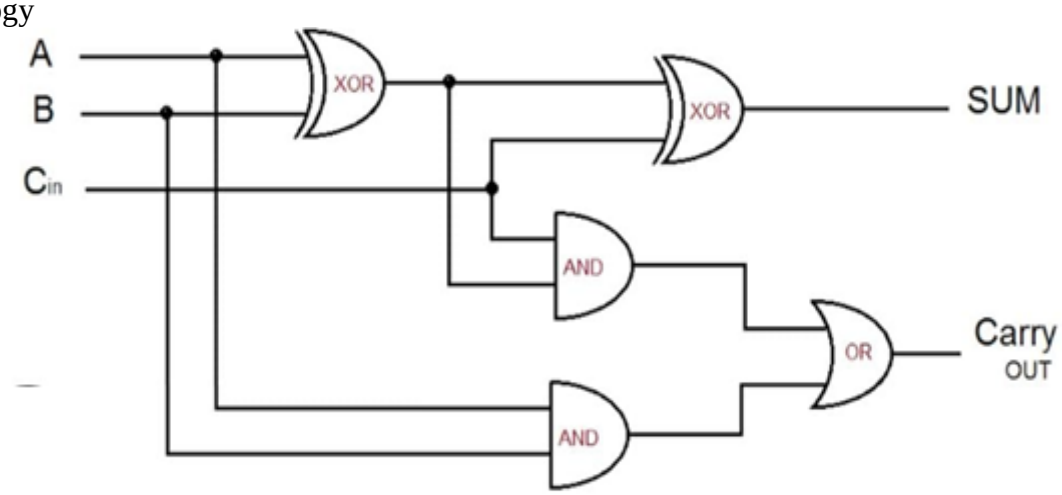

Fig 1. Full adder

2. Existing system

CMOS (complementary metal oxide semiconductor). Static CMOS circuits uses complementary NMOS pulldown and PMOS pull-up networks to implement logic gates or logic functions in integrated circuits. It requires 2N transistors to design a N input logic function. The static power loss is high When the input is '0' then P-MOS will be on and it will charge the output node to vdd. When the input is '1' then N-MOS will be on and the charge stored at the output node get a conducting path

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between output node and ground. Here we used 28- transistor [2] among them 14 P-MOS and 14 N-MOS transistors are used to develop the Full-Adder in C-MOS technology. The power of the full-adder is -9.8135uw

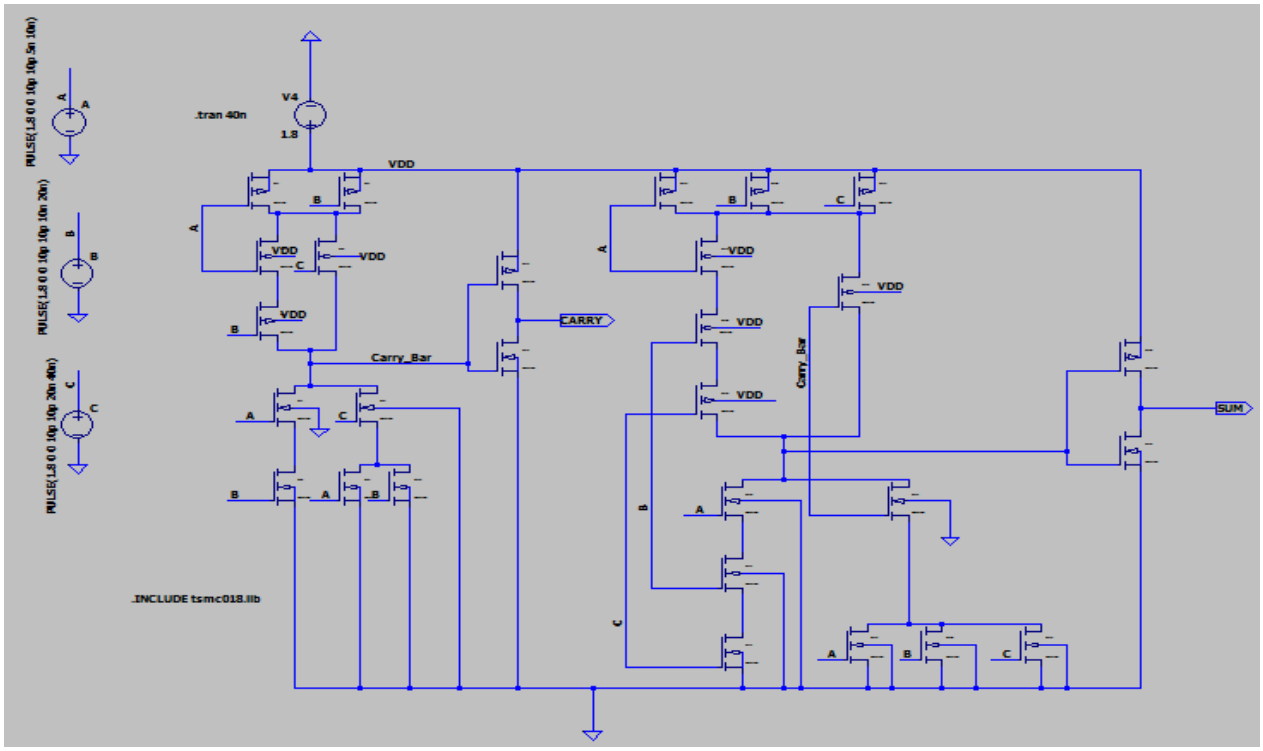

Fig 2. Full adder

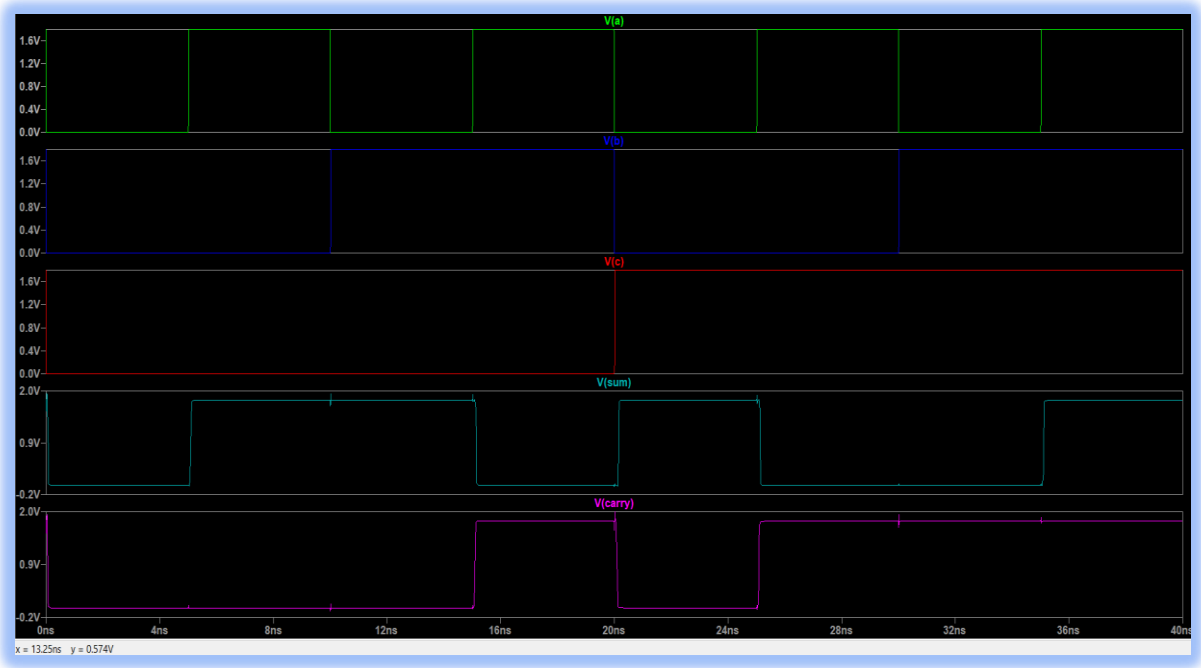

Fig 3. Simulation Result of FA CMOS Logic

3. Dynamic CMOS

Dynamic is an alternative logic style .Which is better than static mode. Its consists of faster switching speeds, no static power consumption ,non-ratioed logic, Full swing voltage levels and less number of transistors. To design an N Input logic function it requires N+2 transistors versus 2N transistors in standard CMOS Logic. High speed is the distinct specification of this Logic It consists of two phases

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pre-charge and evaluation phase. When Clock=0, circuit enters into precharge phase and the output is connected to vdd , when the clock=1,circuit enters into evaluation phase and the output is connected to gnd through NMOS network.

Dynamic CMOS Limitations

It consists of problems like capacitive coupling, charge leakage and charge sharing. Limitation in cascading several stages which is overcome by domino logic. Some excess power is consumed because the circuit has to be precharged after every evaluation. The pull down network takes longer time to evaluate its output. If clock arrives earlier.

4. Proposed system: Domino CMOS logic

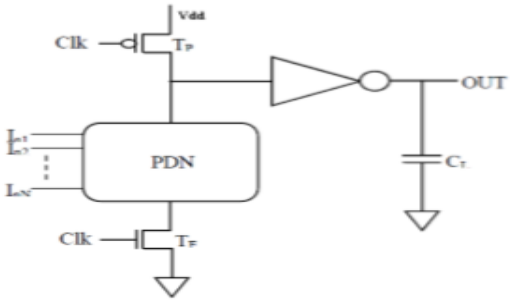

Fig 4. Domino Logic

Domino logic family finds a wide variety of applications. The less transistor count compared to CMOS. The high speed of operation such as microprocessors, dynamic memory, etc. It's an evolution in CMOS-based dynamic logic technique. An inverter is used to avoid the cascading problem in dynamic logic. Requires less area. Here we used the 1.8v and 22 transistors among them 2-transistors are keeper transistors. The keeper transistors are used to overcome the noise. 6-PMOS transistors and 14-NMOS transistors. We designed the full adder by using the mirror logic

Properties of Domino CMOS

- Since each dynamic gate has a static inverter, only non-inverting logic can be implemented.
- Very high speeds can be achieved: only a rising edge delay exists, while tpHL equals zero.
- The inverter can be sized to match the fan-out, which is already much smaller than in the complimentary static CMOS case, as only a single gate capacitance has to be accounted for per fan-out gate

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1 Bit Full adder using Mirror logic

- Implementation using (inversion and duality) properties gives logic
- Any expression that satisfy inversion property also exhibits duality
- principle i.e $AND \leftrightarrow OR$

$$\text{Cout} = AB + Cin(A+B)$$

It's duality is

$$cout = (A+B).(Cin+AB)$$
$$= Acin + Bcin + AAB + ABB$$
$$= Acin + Bcin + AB + AB$$
$$= Acin + Bcin + AB$$
$$Cout = AB + Cin(A+B)$$

i.e $Cout = AB + Cin(A+B) \Leftrightarrow cout = (A+B).(Cin+AB)$

$$Sum = ABCin + \overline{Cout}(A+B+Cin)$$

It's dual is

$$sum = (A+B+Cin)(\overline{Cout} + ABCin)$$
$$= A\overline{Cout} + AABCin + B\overline{Cout} + ABBCin + Cin\overline{Cout} + ABCinCin$$
$$= A\overline{Cout} + B\overline{Cout} + Cin\overline{Cout} + ABCin$$
$$sum = \overline{Cout}(A+B+Cin) + ABCin$$

i. e $sum = ABCin + \overline{Cout}(A+B+Cin) \Leftrightarrow (A+B+Cin)(\overline{Cout} + ABCin)$

Inversion

$$Cout = AB + ACin + BCin \Leftrightarrow \overline{Cout} = \bar{A}\bar{B} + \bar{B}\overline{Cin} + \bar{A}\ \overline{Cin}$$

$$Sum = ABCin + \overline{Cout}(A+B+Cin) \Leftrightarrow \overline{sum} = \bar{A}\bar{B}\overline{Cin} + Cout(\bar{A}+\bar{B}+\overline{Cin})$$

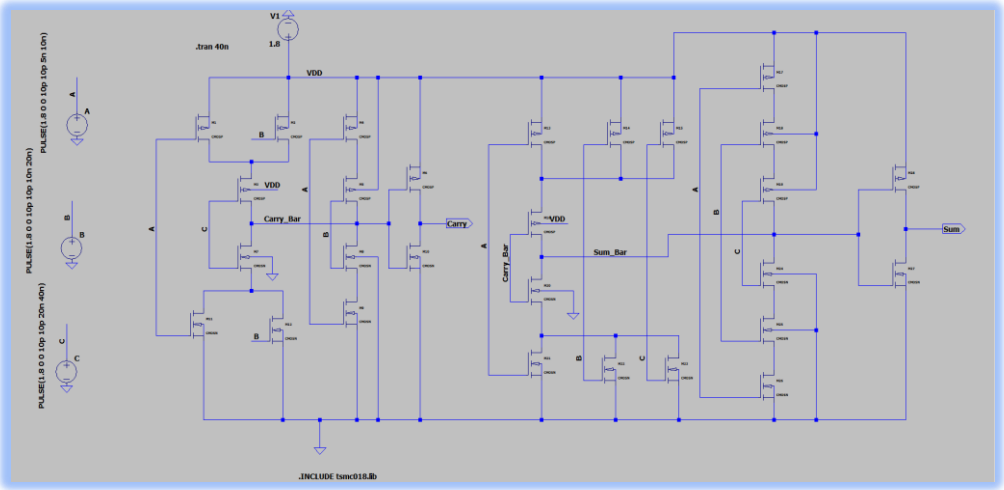

Fig 5. 1-Bit Full Adder (Static CMOS)

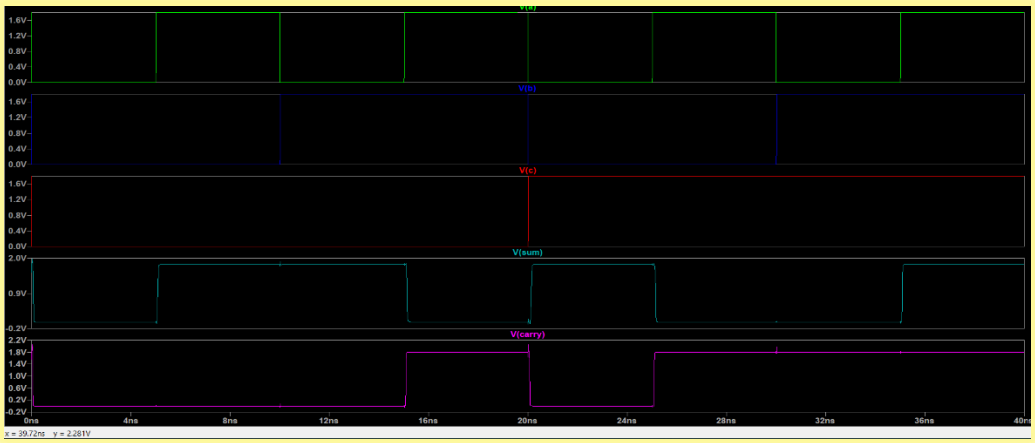

Fig 6. Simulation Result of Static CMOS

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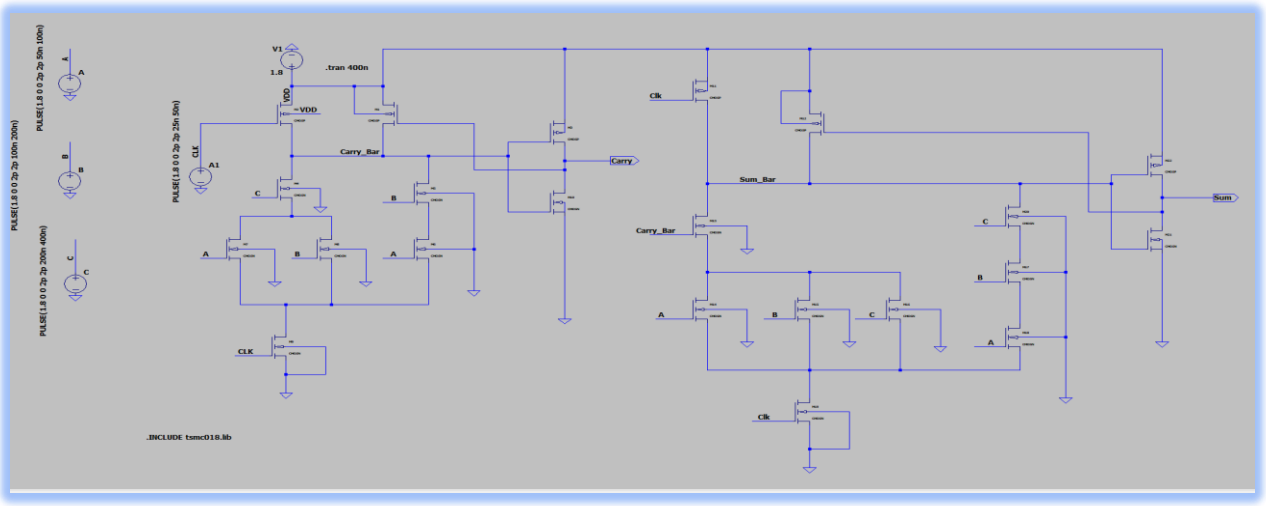

Fig 7. 1-Bit Full Adder (Domino CMOS)

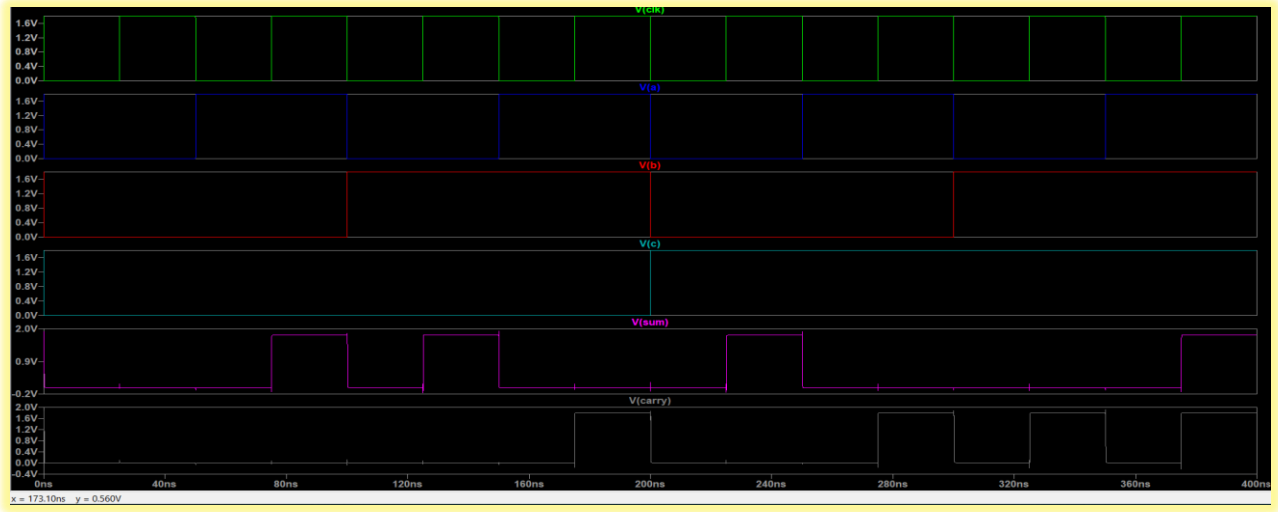

Fig 8. Simulation Result of Domino CMOS

CONCLUSION

In this paper designing of full adder circuit using the CMOS logic and Domino logic has been done. We used LT SPICE software, 180nm technology for analyzing the full adder circuit. It was found that Domino logic gives us very accurate results with less number of transistors and minimum delay as compare to the CMOS design logic. There are almost no glitches in Domino logic transient analysis. Further there is a decrease in chip area by 28.5% and delay by 47.37% in Domino logic as compared to CMOS logic.

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