International Journal of Engineering Technology and Management Sciences
Website: ijetms.in Issue: 2 Volume No.7 March - April – 2023
DOI:10.46647/ijetms.2023.v07i02.041 ISSN: 2581-4621

Design and Implementation of Area Efficient 16-bit Carry Skip Adder

E.Kumar[1], M.Surekha[2], B.Jagadeesh[3], P.Venkata Sai Ramakrishna[4], N.V.S.S Sujith[5], B.Manjunadha[6]

[1]*UG – Electronics and Communication Engineering P.B.R VITS, Kavali, Nellore, A.P*
[2] *Assistant Professor - Electronics and Communication Engineering P.B.R VITS, Kavali, Nellore,A.P*
[3]*UG - Electronics and Communication Engineering P.B.R VITS, Kavali, Nellore, A.P*
[4] *UG - Electronics and Communication Engineering P.B.R VITS, Kavali, Nellore, A.P*
[5] *UG - Electronics and Communication Engineering P.B.R VITS, Kavali, Nellore, A.P*
[6] *UG - Electronics and Communication Engineering P.B.R VITS, Kavali, Nellore, A.P*
Corresponding Author Orcid ID : 0009-0008-1999-6588

ABSTRACT
Adders are fundamental unit in many computer systems. One of the most efficient adder architectures in terms of delay and area is the carry-skip adder. In this paper an area efficient 16-bit carry-skip adder to achieve high speed and low area were designed. CSA is a rapid adder that is used in data processing systems to execute quick arithmetic operations. As a result, a Modified Carry Skip Adder (MCSA) is developed using a single Ripple Carry Adder (RCA) and a Binary to Excess-1 Converter (BEC) instead of twin RCAs to save size while sacrificing speed. The design is coded in VHDL and its area and delay are analyzed using Xilinx ISE 14.7. The hardware simulation is done in Xilinx Spartan 3E FPGA.
Keywords — Carry Skip Adder, Ripple Carry Adder, 5-Bit Excess-1 Converter, 10:5 MUX

1. Introduction

Power consumption is significant factor in designing very large scale integrated (VLSI) circuit. Moreover with the explosive evolution of VLSI technology the demand and popularity of compact devices has driving designers to struggle for smaller silicon area. The fundamental electronic circuit used for addition is adder. Adders are important in digital system. Many adders are exist but the fast adding with Low area and Power still interesting. There are different types of adders such as Ripple carry adder (RCA),carry skip adder (CSKA), carry look ahead adder (CLA), carry save adder (CSLA), etc. among them RCA shows compact design but their computation time is high. It has lowest speed among all adder because it has huge propagation delay but occupy less area. Then, in CLA can derive fast result but it leads to increase in area, among these adders CSLA have small area but delay is increased due to ripple carry adder. In this paper an area efficient 16-bit carry-skip adder to achieve high speed and low area were designed. CSA is a rapid adder that is used in data processing systems to execute quick arithmetic operations. As a result, a Modified Carry Skip Adder (MCSA) is developed using a single Ripple Carry Adder (RCA) and a Binary to Excess-1 Converter (BEC) instead of twin RCAs to save size while sacrificing speed.

To add an N-bit number, N number of adder circuits can be cascaded all together. There must be N complete adder circuits for an N-bit parallel adder. A ripple carry adder is a logic circuit in which the carry-out of each full adder is equal to the carry-in of the next full adder. Since each carry bit is rippled into the next full adder, it is called a ripple carry adder or parallel adder. In a ripple carry adder, the sum and carry out bits of each full adder stage are inacceptable until the stage's carry in happens. This is due to propagation delays inside the logic circuitry.

International Journal of Engineering Technology and Management Sciences
Website: ijetms.in Issue: 2 Volume No.7 March - April – 2023
DOI:10.46647/ijetms.2023.v07i02.041 ISSN: 2581-4621

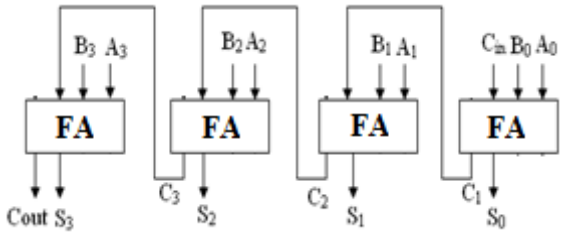

Fig 1. Ripple Carry Adder

Carry skip adder is a fast adder used in digital as well as memory architectures. Individual ripple carry adder's Carry will be '0,' and '1'. The output sum and carry are recognised by the 2 to 1 multiplexers in this case. Carry can be used to represent the multiplexer's control signal (Cin)

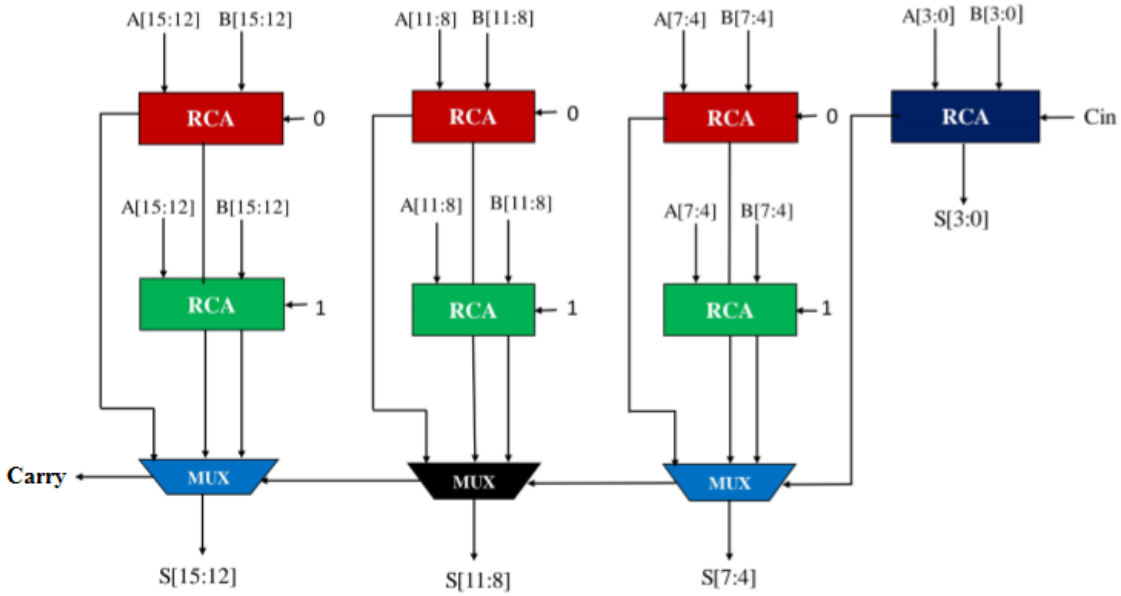

Fig 2.16-bit Carry Skip Adder

Carry Skip adders are classified into two types: uniform and variable sized adders. A uniform sized adder is one that divides the bit length consistently. The linear Carry Skip adder is another name for it. Bit lengths in variable sized adders are normally unequally split.

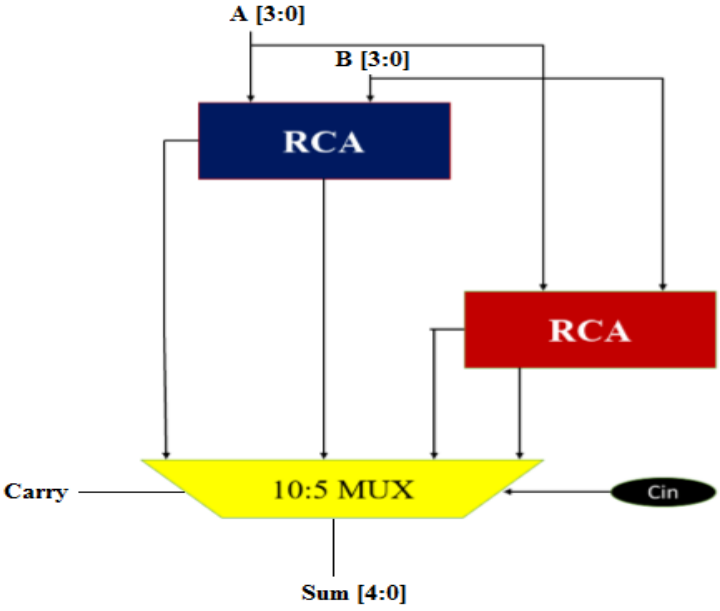

Fig 3. Carry Skip Adder using 10:5 Multiplexer

International Journal of Engineering Technology and Management Sciences
Website: ijetms.in Issue: 2 Volume No.7 March - April – 2023
DOI:10.46647/ijetms.2023.v07i02.041 ISSN: 2581-4621

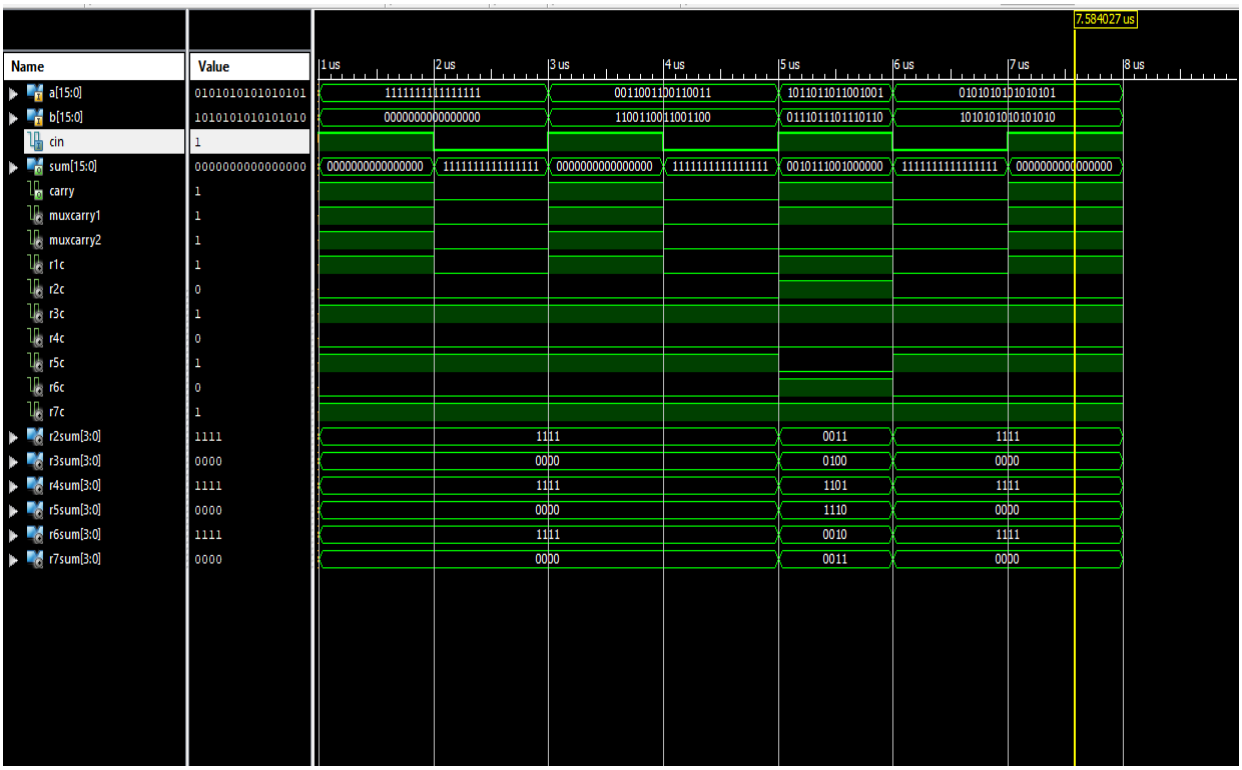

Fig 4. Simulation Result Of 16-bit Carry Skip Adder

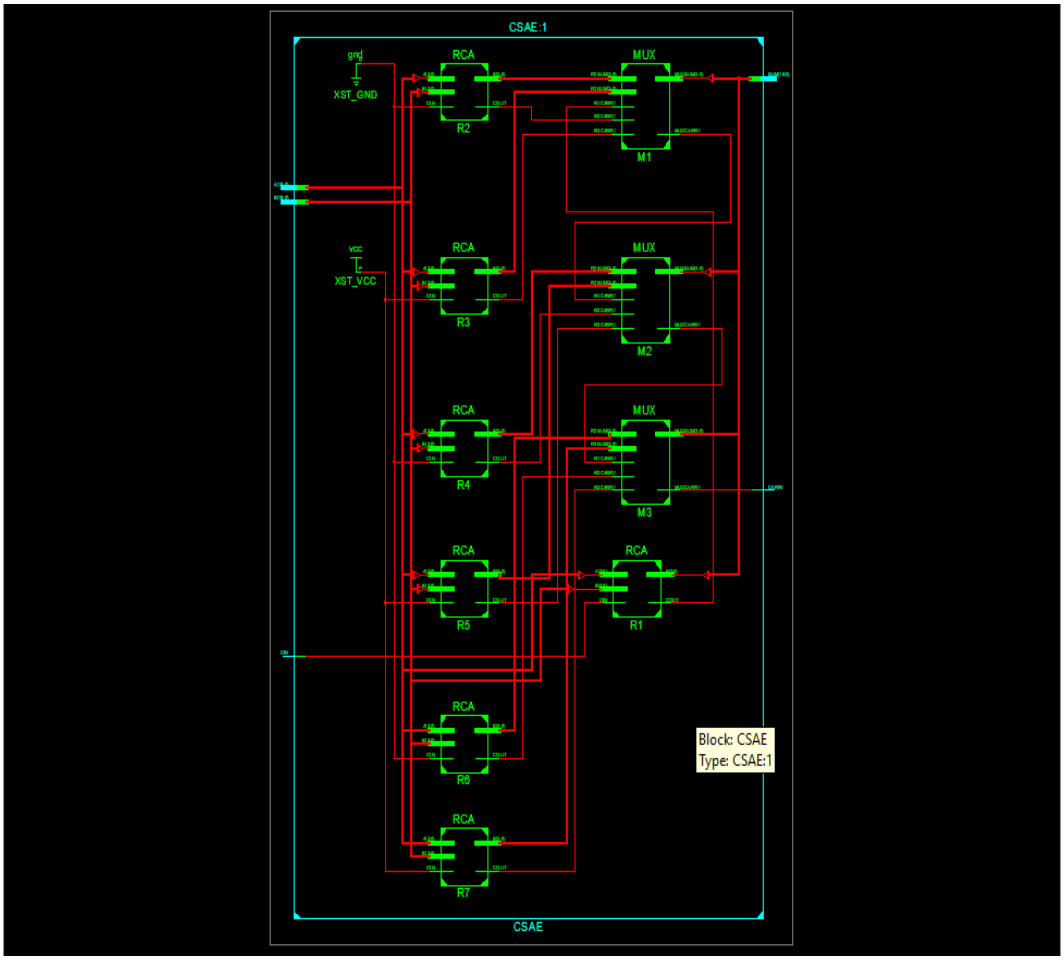

Fig 5. RTL Schematic of 16-bit Carry Skip Adder

International Journal of Engineering Technology and Management Sciences
Website: ijetms.in Issue: 2 Volume No.7 March - April – 2023
DOI:10.46647/ijetms.2023.v07i02.041 ISSN: 2581-4621

2. Proposed system

The proposed structure of Modified Carry Skip adder employs single RCA and 5 bit Binary to excess one converter instead of dual Ripple carry adder to decrease size and power consumption. The reason for the lesser space 5 bit binary to excess one converter has less logic gates than the ripple carry adder. As a result, there is a significant decrease in silicon area, and modified carry skip adder is constructed for a large number of bits.

5 bit Binary to excess-1 converter

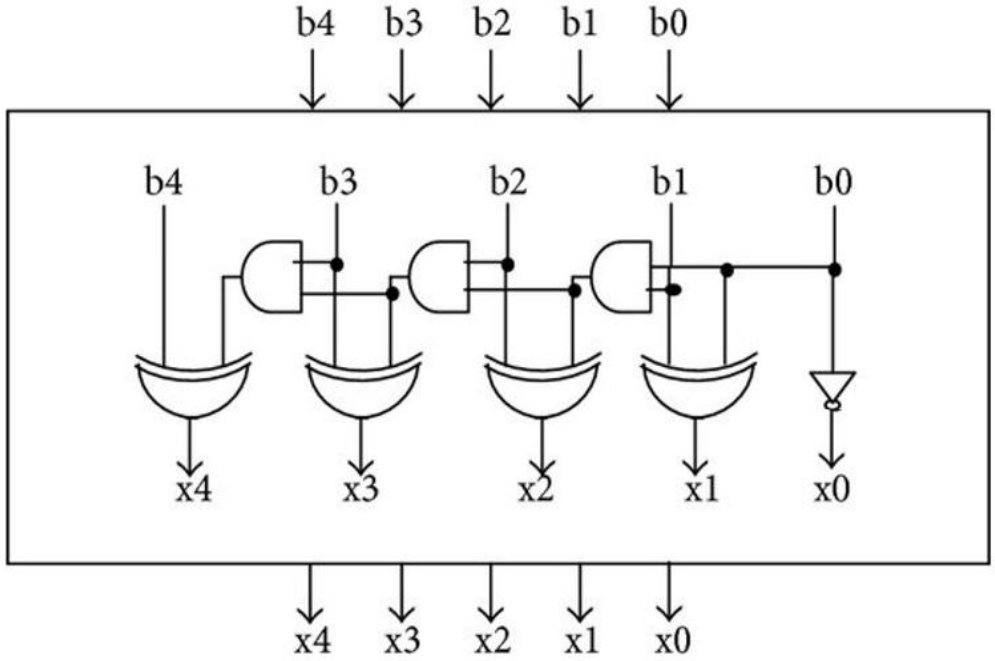

Fig 5. 5-bit Binary to excess one converter

Binary to Excess-1 Converter (BEC) is used in place of RCA with Cin=1 to lower the size and power consumption of traditional CSA. N+1 bit BEC is used to replace the N-bit RCA. The advantage of BEC is that it employs fewer logic gates than the N-bit full adder configuration.

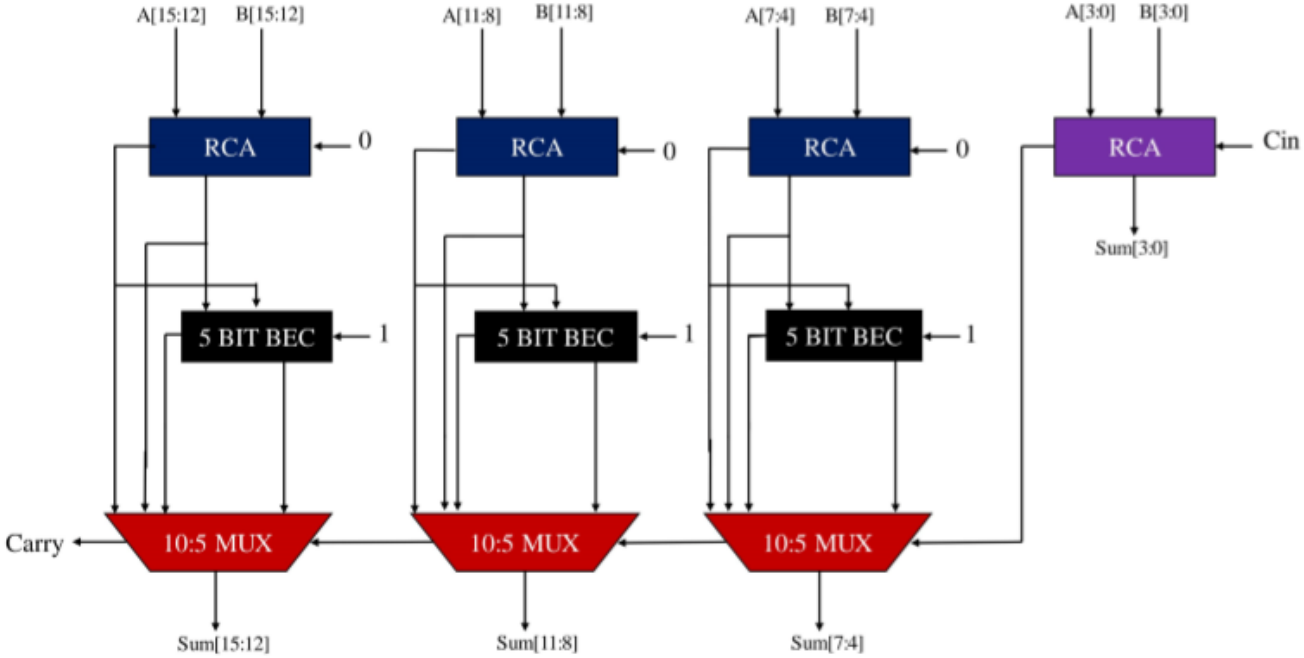

Fig 6. 16-bit Modified Carry Skip Adder

International Journal of Engineering Technology and Management Sciences
Website: ijetms.in Issue: 2 Volume No.7 March - April – 2023
DOI:10.46647/ijetms.2023.v07i02.041 ISSN: 2581-4621

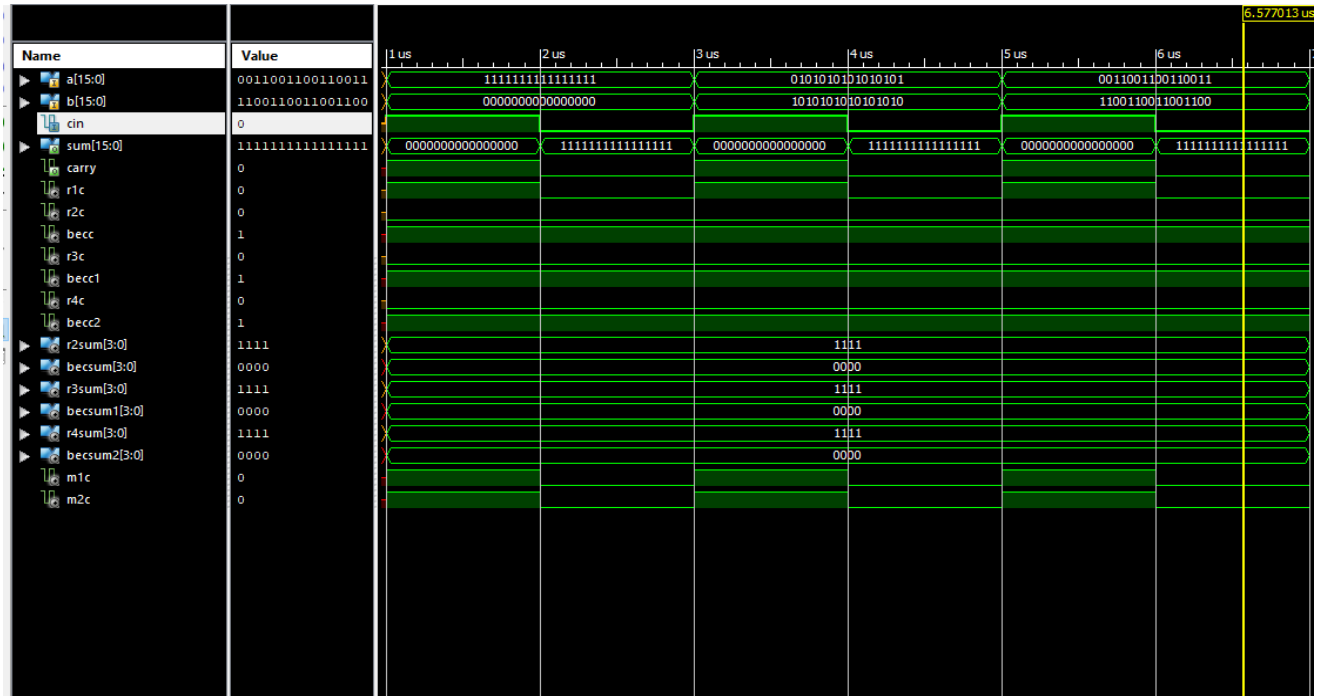

Fig 7. Simulation Result of 16-bit Modified Carry Skip Adder

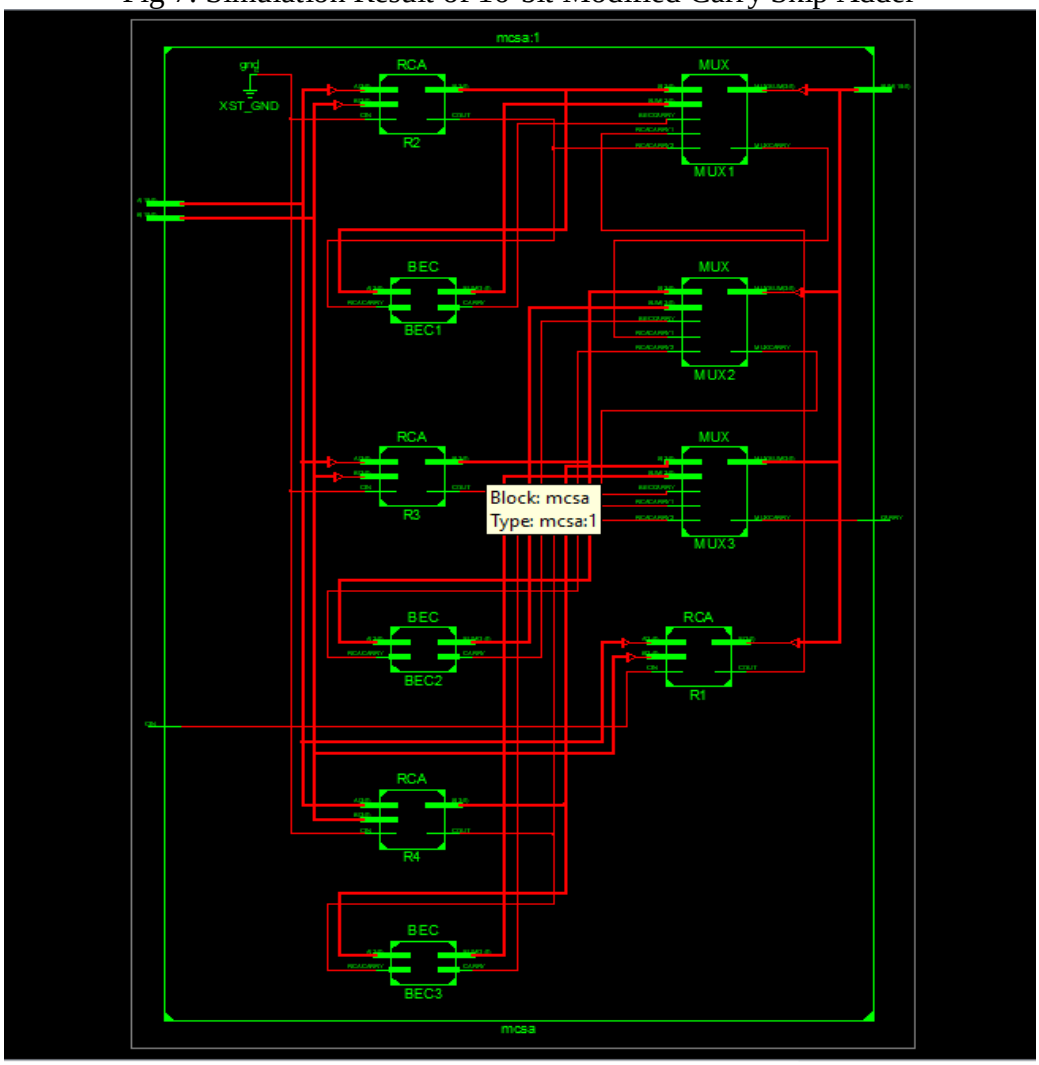

Fig 8. RTL Schematic of 16-bit Modified Carry Skip Adder

DOI:10.46647/ijetms.2023.v07i02.041 ISSN: 2581-4621

3. CONCLUSION

With minimal size and power usage, an efficient modified Carry Skip adder for 8-bit, 16-bit, 32-bit, and 64-bit has been suggested utilising a single RCA with Cin=0 and BEC with Cin=1. Although MCSA's latency is somewhat enhanced, a design with reduced size and power consumption is developed. MCSA has a higher frequency than standard CSA.

References

1. B. Ramkumar, Harish M Kittur "Low power and Area efficient carry select adder,"IEEE Trans,Vol.20,Feb 2012.
2. Shivani Parmar and Kirat pal Singh,"Design of high speed hybrid carry select adder", IEEE 2012.
3. Garish Kumar Wadhwa, Amit Grover, Neeti Grover and Gurpreet singh," An Area-Efficient Carry Skip adder Design by using 180nm Technology", International Journal of Advanced Science and Applications, Vol. 4, No. 1,2013.
4. Behnam Amelifard, Farzan Fallah and Massoud Pedram, "Closing the gap between Carry Skip adder and Ripple Carry Adder: a new class of low-power high-performance adders", Sixth International Symposium on Quality of Electronic Design, pp.148- 152. April 2005.
5. J. M. Rabaey, "Digital Integrated Circuits- A Design Perspective", New Jersey, Prentice-Hall, 2001. [5] T.- Y. Chang and M.-J. Hsiao" Carry-Select Adder using single Ripple-Carry Adder", Electronics letters, vol.34, pp.2101-2103, October 1998.
6. T. Y. Ceiang and M. J. Hsiao,"Carry-select adder using single ripple carry adder", Electron Let, vol.34,no.22,oct-2013.
7. Shivani Parmar and Kirat Pal Singh,"Design of High Speed Carry Skip adder", IEEE, 2012.
8. Yuke Wang, C. Pai, and Xiaoyu Song, „"The design of hybrid Carry-Look ahead/ Carry–Select Adders"", IEEE transaction on Circuits and Systems II: Analog and Digital Processing, vol.49, pp.16-24, January 2002.
9. Youngjoon Kim and Lee-Sup Kim, "64-bit carryselect adder with reduced area", Electronics Letters, vol.37, issue 10, pp.614-615, May 2001.
10. Youngjoon Kim and Lee-Sup Kim, "A low power Carry Skip adder with reduced area", IEEE International Symposium on Circuits and Systems, vol.4, pp.218-221, May 2001.
11. Ms. S.Manjui, Mr. V. Sornagopae, " An Efficient SQRT Architecture of Carry Select Adder Design by Common Boolean Logic" ,IEEE, 2013.
12. U,Sreenivasulu and T.Venkata Sridhar, "Implementation of an 4-bit ALU using Low power and Area efficient carry select adder ", International Conference on ELECTRONICS AND Communication Engineering,20 May2012.
13. B.Ramkumar, Harish M Kittur and P.Mahesh Kannan, "ASIC implementation of Modified Faster Carry Save Adder", European Journal of Scientific Research, vol.42, pp.53-58, 2010.
14. Kuldeep Rawat, Tarek Darwish and Magdy Bayoumi, "A low power and reduced area Carry Skip adder", 45th Midwest Symposium on Circuits and Systems, vol.1, pp. 467- 470, March 2002.
15. R.Uma, Vidya Vijayan, M.Mohanapriya, Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies", International Journal of VLSI Design & Communication Systems, Vol. 3, No. 1, pp. 153-168, Feb 2012.