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Fabrication of CNTFET Simulation Using Cadence Virtuoso

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Abstract
In this paper, the fabrication of CNTFET with the help of simulation using cadence virtuoso is presented. The process of fabricating Carbon Nanotube Field-Effect Transistors (CNTFETs) is a sophisticated task that demands great attention to detail. To aid in the design and optimization of CNTFET fabrication processes, simulation tools are often utilized. CNTFET fabrication simulations generally involve modeling the physical and chemical processes of creating the carbon nanotube channel, as well as the device's metal contacts and other components. Simulation tools such as COMSOL Multiphysics or Lumerical are used to model the mechanical, thermal, and electrical properties of the materials involved, and to predict how they will behave during fabrication. An essential challenge in CNTFET fabrication is obtaining precise control over the nanotube placement and orientation, which can be addressed through modeling the nanotube growth and optimizing the growth parameters to achieve the desired properties. Furthermore, simulations can assist in optimizing the process parameters for depositing metal contacts on the nanotubes, which is critical for achieving good device performance. Overall, simulation tools play a vital role in the CNTFET fabrication process, enabling researchers to optimize the device design and fabrication parameters for improved performance and yield. The work done & presented in this paper is the result of the mini-project work that has been done by the first sem engineering students of the college and as such there is little novelty in it and the references are being taken from various sources from the internet, the paper is being written by the students to test their writing skills in the starting of their engineering career and also to test the presentation skills during their mini-project presentation. The work done & presented in this paper is the report of the assignment / alternate assessment tool as a part and parcel of the academic assignment of the first year subject on nanotechnology & IoT.
Keywords: Carbon, Nanotube, FET, Cadence, Virtuoso, Simulation

Introduction

The fabrication of Carbon Nanotube Field-Effect Transistors (CNTFETs) is a complex process that requires careful attention to detail. Simulation tools can be used to aid in the design and optimization of CNTFET fabrication processes [1]. In general, CNTFET fabrication simulations involve modeling the physical and chemical processes involved in creating the carbon nanotube channel, as well as the metal contacts and other components of the device. Simulation tools such as COMSOL Multiphysics or Lumerical can be used to model the mechanical, thermal, and electrical properties of the materials involved, and to predict how they will behave during the fabrication process [2]. One key challenge in CNTFET fabrication is achieving a high degree of control over the nanotube placement and orientation. Simulation tools can be used to model the growth of the nanotubes and to optimize the growth parameters to achieve the desired properties. In addition, simulations can help to optimize the process parameters for depositing metal contacts on the nanotubes, which is critical for achieving good device performance. Overall, simulation tools are an important part of the CNTFET fabrication

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process, helping researchers to optimize the device design and fabrication parameters for maximum performance and yield [3].

Proposed methodology & block diagram

The fabrication of a carbon nanotube field-effect transistor (CNTFET) simulation using Cadence Virtuoso involves several steps: Design the CNTFET layout: Using a layout editor in Cadence Virtuoso, create the physical layout of the CNTFET. This includes the CNT channel, the metal source and drain contacts, and any necessary interconnects. Generate the netlist: Using a schematic editor, create a circuit schematic that represents the CNTFET design [4]. Once the schematic is complete, use Cadence Virtuoso's netlist generator to create a netlist file that represents the connectivity of the circuit. Create the simulation setup: In Cadence Virtuoso's Analog Design Environment (ADE), set up the simulation parameters, including the type of analysis (DC, AC, transient, etc.), the simulation options, and any input or output signals. Run the simulation: Once the simulation setup is complete, run the simulation in ADE [5]. The simulation results can be viewed in various formats, including waveform plots and numerical data. Analyze the simulation results: After the simulation is complete, analyze the results to determine the performance of the CNTFET. This may include measurements such as the device current-voltage characteristics, transconductance, and gate capacitance. Optimize the design: Based on the simulation results, make any necessary changes to the CNTFET layout or circuit schematic to optimize its performance. This may involve iterating through steps 1-5 until the desired performance is achieved [6].

Simulation Results

The V-I characteristic graph of a CNTFET typically exhibits two regions of operation: the linear region and the saturation region. In the linear region, the device behaves as a resistor, and the current is proportional to the applied voltage. In the saturation region, the current becomes independent of the drain-source voltage due to the formation of a depletion region near the drain. The V-I characteristic graph of a CNTFET is affected by several factors, including the number of carbon nanotubes in the channel, the diameter of the carbon nanotubes, and the contact resistance between the carbon nanotubes and the metal source / drain electrodes. The Figs. 1 to 3 gives the cadence circuit design layout view @ different stages of the design process [7].

Advantages

Time and cost savings: Fabricating physical prototypes of CNTFETs can be time consuming and expensive. By using simulations, researchers and engineers can evaluate multiple designs and performance parameters without the need for physical fabrication, which can save time and resources. Design optimization: By adjusting the device's physical structure or circuit design based on simulation results, researchers can refine their designs to achieve higher performance and efficiency. CNTFETs, show different characteristics compared to MOSFETs in their performances. CNTFETs have high gate power and improved Channel transport. The CNT conducts on its surface where all the chemical bonds are saturated and stable. Therefore, CNTFETs are more stable compared to MOSFETs [8].

Applications

- Circuit design and optimization: CNTFET simulations can be used to design and optimize the performance of circuits that use CNTFETs, such as amplifiers, logic gates, and memory devices.
- Material characterization: Simulation results can be used to evaluate the impact of various factors, such as the diameter and chirality of the nanotubes, on their electronic behavior and mechanical properties of devices.
- Education and training: CNTFET simulations ca]n be used to educate and train students and researchers in the design and analysis of nano electronic devices

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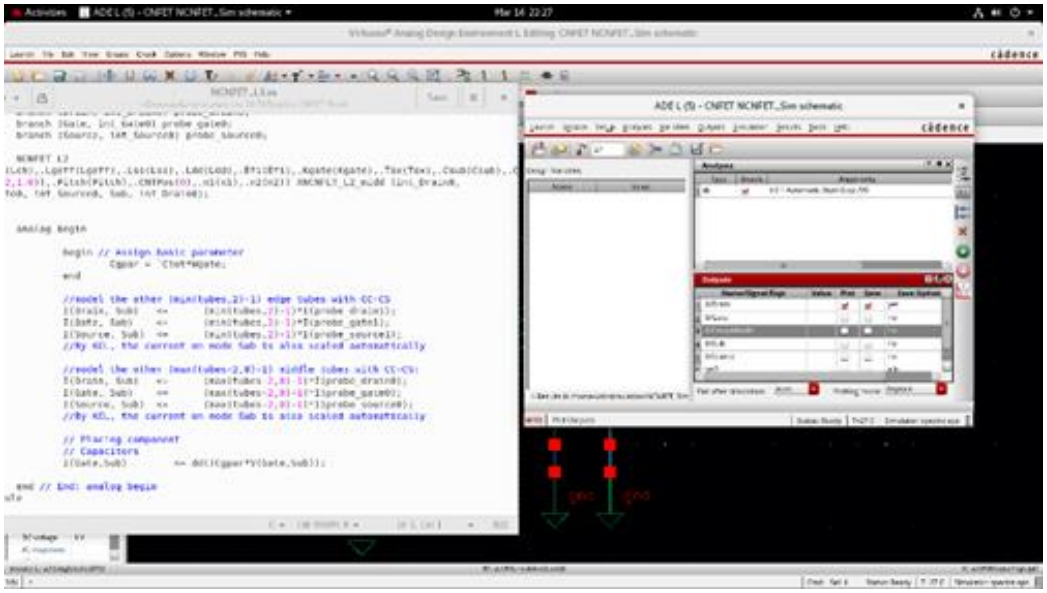

Fig. 1 : Cadence circuit design layout view - 1

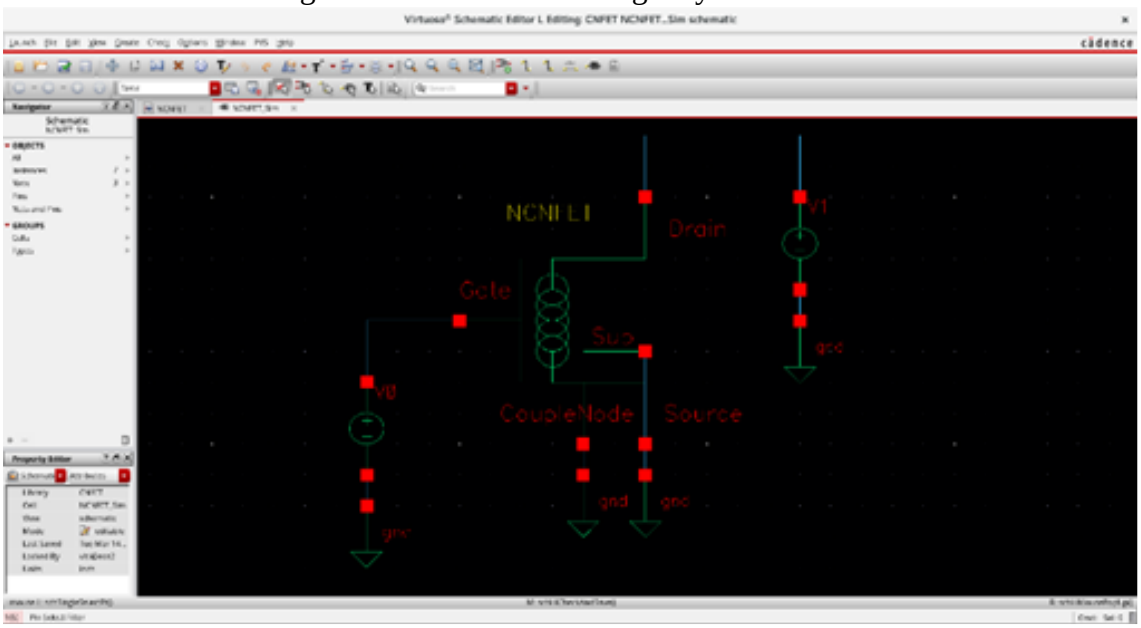

Fig. 1 : Cadence circuit design layout view - 2

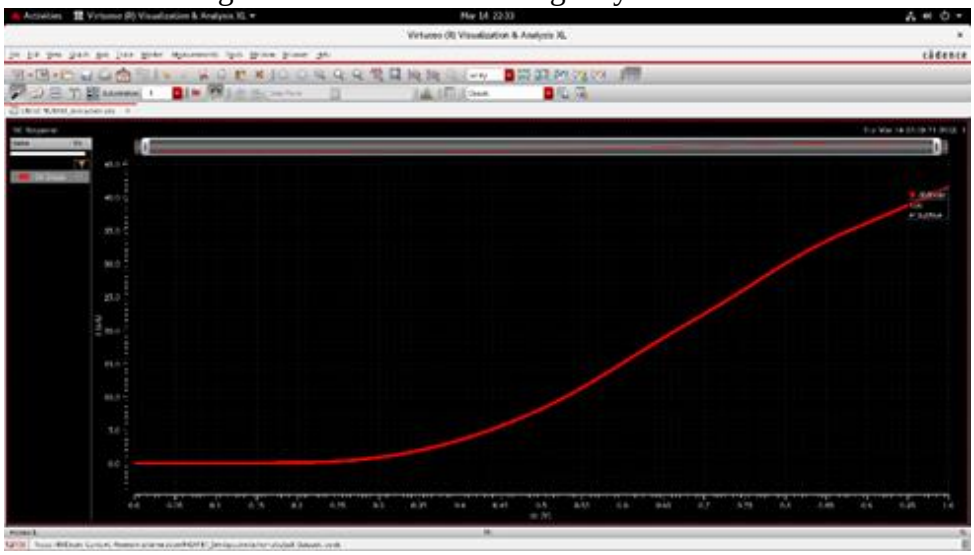

Fig. 1 : Cadence circuit design layout view - 3

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Conclusions

Overall, simulation of CNTFET fabrication using Virtuoso can provide valuable insights into device behavior and performance, helping in the design and optimization of these devices for various applications.

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