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Design of Area efficient comparator architecture using 5T XOR GATE

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Abstract
The use of comparators in computation-based designs is extensive, making optimization crucial. While some comparator designs use dynamic logic to achieve low-power consumption, the limitations of low-speed and poor-noise margin make this approach challenging. The proposed comparator design offers a new solution that is both area-efficient and has a high operating speed while consuming low-power. It was designed using 180nm technology in Tanner Tool, and its results were observed. Overall, this work presents a promising new solution for optimizing digital comparators and improving the efficiency and speed of computation-based designs. This work presents a new solution for optimizing N-bit digital comparators in terms of area, power, and speed. The proposed comparator structure is a clever design that consists of two crucial modules - the comparison evaluation module (CEM) and the final module (FM). The CEM is responsible for evaluating the comparison, and it uses a regular structure of repeated logic cells to implement a parallel prefix tree structure. This approach is independent of input operand bit widths, which makes it highly versatile and adaptable to different applications. The FM, on the other hand, validates the final comparison based on the results obtained from the CEM. This ensures that the final output is accurate and reliable. By utilizing these two modules, the proposed comparator structure is able to achieve high-precision comparisons while maintaining a relatively simple and efficient design. Overall, this comparator structure is a promising development in the field of digital circuit design, and it has the potential to improve the performance and reliability of a wide range electronic systems.

I. INTRODUCTION

Digital comparators are indeed a critical component in the design of numerous electronic applications. They are essential in scenarios where the output depends on the results obtained from computational comparison activities. Such applications include digital image processing, pattern recognition/matching, arithmetic sorting, data compression, and digital neural networks, among others. In digital image processing, for instance, digital comparators are used to compare pixel values to determine the presence of specific features such as edges, corners, and shapes. In pattern recognition and matching, comparators are used to match patterns by comparing their features. In data compression applications, comparators are used to identify and eliminate redundant data, thus reducing the size of the data being transmitted or stored. Similarly, in digital neural networks, comparators play a fundamental role in the computation of neuron activation functions. Overall, the importance of digital comparators in modern electronic systems cannot be overstated. Their ability to perform accurate and reliable comparisons plays a critical role in various applications, making them an indispensable design element in the digital world. They also find use in test circuit applications such as built-in self-test circuits, signature analysers and jitter measurement, with comparators being a basic design element. Optimizing the design of comparators is crucial as they are extensively used in various computation-based designs, with the need to optimize in terms of area, power, and speed. However, optimized comparator designs are still used as a key component in general-purpose computer architecture for developing memory addressing logic, queue buffers, test circuits, and more. Overall, digital comparators are an essential building block in many digital systems and their optimization is crucial for improving the efficiency and performance of these systems.

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a) Existing Work

The existing method uses a 7t XOR in the comparator circuit to provide full swing voltage. The N-bit digital comparator is shown in Figure 1 and is divided into two modules - the comparison evaluation module (CEM) and final module (FM). These modules provide high-level and low-level architectures for the comparison process. The CEM uses a parallel prefix tree structure to perform bitwise comparison of two N-bit operands A and B, represented by AN-1AN-2...A0 and BN-1BN-2...B0.To explore the regularity of the comparator for arbitrary bit widths, the two operands A and B are divided into 4-bit partitions as AN-1AN-2AN-3AN-4...A3A2A1A0 and BN-1BN-2BN-3BN-4...B3B2B1B0. The comparison process is divided into five sets, with sets 1-4 contained within the comparison evaluation module (CEM) and set 5 contained within the final module (FM). The sets are organized in four hierarchical prefix orders based on their functionality. The output of each set serves as the input of another set, except for set 1, whose outputs act as the inputs of sets 2 and 3. This organization allows for efficient and effective comparison of N-bit binary operands. Set 1 performs the bitwise comparison of two N-bit binary operands using a novel EX-OR-NOR cell. The proposed structure of the EX-OR-NOR cell is based on pass transistor logic and CMOS logic. It uses only seven transistors, compared to the conventional eight-transistor model, for both EX-OR and EX-NOR operations.

b) Proposed Work

The increasing demand for portable electronics has led to a need for smaller silicon area, higher speeds, longer battery life, and greater reliability. One important resource that designers try to conserve is power. Full adders are crucial components in various circuits used for arithmetic operations, including compressors, comparators, and parity checkers. Since full adders are often in the critical paths of complex arithmetic circuits, improving their performance can have a significant impact on the overall system performance. In particular, magnitude CMOS circuits are used to design adders that consume less power while maintaining high-speed operation and smaller size. These circuits are ideal for high-speed interface applications and other power-sensitive applications.

In addition to magnitude CMOS circuits, designers use other techniques such as low-power design methodologies, voltage scaling, and threshold voltage control to reduce power consumption in digital circuits. These techniques help to ensure that the digital circuits consume less power while maintaining optimal performance.

The proposed low power hardware-efficient comparator using 5T XNOR is an excellent example of a technique that addresses the need for hardware efficiency and low power designs in VLSI. The comparator is designed to operate at a low voltage, reducing power consumption, while maintaining high-speed operation. This makes it an ideal solution for applications that require high-speed operation while minimizing power consumption.

In conclusion, the design and analysis of adders and other digital circuits at the circuit level is essential for achieving optimal performance in digital systems. Designers use various techniques and technologies, such as magnitude CMOS circuits and low-power design methodologies, to optimize the performance of digital circuits. The proposed low power hardware-efficient comparator using 5T XNOR is an excellent example of a technique that addresses the need for hardware efficiency and low power designs in VLSI.

The 5T XOR gate is designed to provide optimal output voltage with less area and power consumption, while reducing parasitic effects and maintaining symmetry between power and speed at different voltage levels. Comparators play a crucial role in CPUs, error detection circuits, and microcontrollers, and the XOR gate is a key component in some combinational circuits and encryption and arithmetic circuits. The replacement of the XOR gate with a 4T XNOR in this paper is expected to reduce power and hardware utilization.

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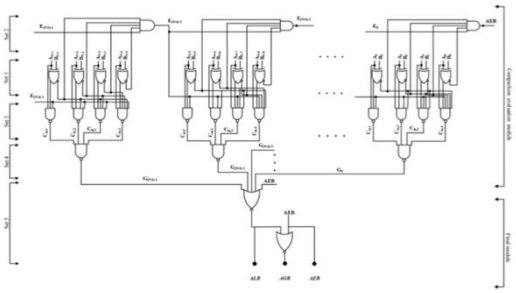

Figure:1 Circuit Diagram of comparator

In designing n-bit comparators, it is important to note that the size of the comparator is directly proportional to the number of XOR gates required, which is n. The power consumption of the XOR gates largely determines the power consumption of the comparator. Therefore, it is necessary to design low power XOR gates to reduce the overall power consumption of the comparator. There are various techniques and technologies used to design low power XOR gates. One such technique is the use of adiabatic logic, which aims to reduce power consumption by minimizing switching activity. The adiabatic XOR gate uses a charging and discharging process to ensure that no current flows between the power source and ground during the switching phase, thus reducing power dissipation. Another technique is the use of pass-transistor logic, which utilizes transmission gates to perform XOR operations. This technique reduces the transistor count and enables the use of smaller transistors, resulting in lower power consumption. Moreover, the use of gate-level voltage scaling techniques is also effective in reducing the power consumption of XOR gates. In this technique, the supply voltage of the XOR gate is lowered, which results in a reduction of power consumption. However, this technique requires careful analysis and design to ensure that the logic function is still correctly performed at the lower voltage level. Overall, utilizing these low power design techniques can significantly reduce the power consumption of XOR gates, which in turn reduces the power consumption of n-bit comparators.

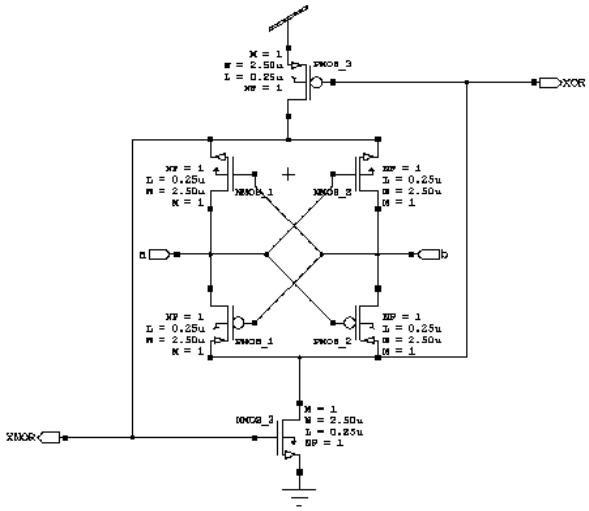

Figure :2 5T XOR GATE

The proposed XOR gate design not only provides better power and area efficiency but also offers full swing voltage and good driving capability. This is a significant advantage as it allows the XOR gate to be cascaded to any number of stages without suffering from a degradation of voltage levels or driving capability. The full swing voltage capability ensures that the output voltage of the XOR gate covers the entire voltage range, which enables it to drive other circuits with different voltage levels. Additionally, the good driving capability ensures that the XOR gate can drive multiple loads without significant signal degradation or voltage drop.

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The cascading of XOR gates is a common technique used in designing n-bit comparators. By cascading several XOR gates, it is possible to create a multi-bit comparator that can compare two n-bit numbers. The good driving capability of the proposed XOR gate design means that it can be cascaded to any number of stages without suffering from voltage level degradation or signal loss .Overall, the proposed XOR gate design offers several advantages over traditional designs, including better power and area efficiency, full swing voltage capability, and good driving capability. These advantages make it a suitable choice for use in n-bit comparators and other digital circuits that require efficient and reliable operation.

II. RESULTS

	Power(mw)	delay	area
Proposed 64 bit comparator	4.6	4.3	1318
Exist 64bit comparator	5.6	4.3	1382
proposed 24bit comparator	1.7	1.2	498
Exist 24bit comparator	1.9	1.2	522
Proposed 16bit comparator	4.9	0.6	334
Exist 16bit comparator	6.8	0.3	350

Figure:3 Comparison Table

```
* General options:
*             temp = 25 [deg C]          threads = 4
*
* Output options:
*            acout = 1                    ingold = 0
*


*  Device and node counts:
*              MOSFETs - 1318              MOSFET geometries - 6
*                  BJTs - 0                          JFETs - 0
*              MESFETs - 0                           Diodes - 0
*           Capacitors - 0                       Resistors - 0
*            Inductors - 0                  Mutual inductors - 0
*  Transmission lines - 0        Coupled transmission lines - 0
*     Voltage sources - 129              Current sources - 0
*                VCVS - 0                          VCCS - 0
*                CCVS - 0                          CCCS - 0
*    V-control switch - 0               I-control switch - 0
*       Macro devices - 0        External C model instances - 0
*         HDL devices - 0
*         Subcircuits - 0          Subcircuit instances - 178
*   Independent nodes - 595              Boundary nodes - 130
*         Total nodes - 725
```

Figure:4 Represents Area of 64bit comparator

```
MEASUREMENT RESULTS

DELAY = 4.3294e-009
   Trigger = 1.0020e-008
   Target  = 1.4349e-008

* END NON-GRAPHICAL DATA
```

Figure:5 Delay

```
* BEGIN NON-GRAPHICAL DATA

Power Results
Vl from time 0 to 1e-007
Average power consumed -> 4.653711e-003 watts
Max power 4.956402e-002 at time 8.0776e-008
Min power 9.015814e-008 at time 1e-008
```

Figure:6 power

CONCLUSION

The paper describes the design and implementation of a novel 5TXOR gate, which is utilized in a proposed comparator design. The comparator is designed using CEM (Carry-Select Adder-based Extended Modified) and FM (Fowler-Martin) structures. The proposed comparator design offers several advantages over existing comparators designed using 0.18 µm CMOS technology. The 5TXOR gate utilized in the proposed comparator design offers several benefits, including reduced power consumption and improved area efficiency. The novel design of the 5TXOR gate enables it to be used in a wide range of applications, including adders, multipliers, and other digital circuits. Overall, the proposed comparator design utilizing the 5TXOR gate and CEM/FM structures

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represents a significant improvement over existing comparator design. Its improved performance and efficiency make it a suitable choice for various applications in the field of digital circuit design.

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