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A Novel Implementation of QPSK Modulator on FPGA

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ABSTRACT
QPSK is one of the digital modulation techniques in communication system that has wide applications in the field of wireless, satellite communication, Bluetooth, OFDM etc. The Conventional QPSK modulators designs are generally based on IQ approach. In these modulators multipliers are used to separate the modulating signal into the in-phase and quadrature phase which increases the hardware complexity. The objective of this work is to implement the digital QPSK modulator with conventional and another approach of digitization. In this approach a digitized carrier wave is generated and QPSK phase shifting is provided by 4:1 multiplexer according to the data bits. The implementations of both the designs are done on Spartan 3E Xilinx FPGA through the verilog hardware description language. The QPSK modulator based on the Digitized approach is simpler in terms of hardware circuitry.
Keywords— Quadrature Phase Shift Keying (QPSK); Deterministic Random Bit Generator (DRBG); Verilog; Look up table (LUT); FPGA; Serial in Parallel out (SIPO).

1. Introduction :

Modulation is phenomena in which characteristic like amplitude, phase and frequency of a high frequency carrier wave is changed accordingly low frequency modulating wave. Modulation is required to minimize the noise in signal and to separate the signal from different transmitters. Generally, Modulation can be done by two ways the analog and digital modulation.Digital modulation provides more information capacity, greater noise immunity, robustness to channel impairments, higher data security, better quality communication, compatibility with digital data service.Faster system availability and easier multiplexing of various forms of information like voice, data and video etc.

2. Experimental Methods or Methodology

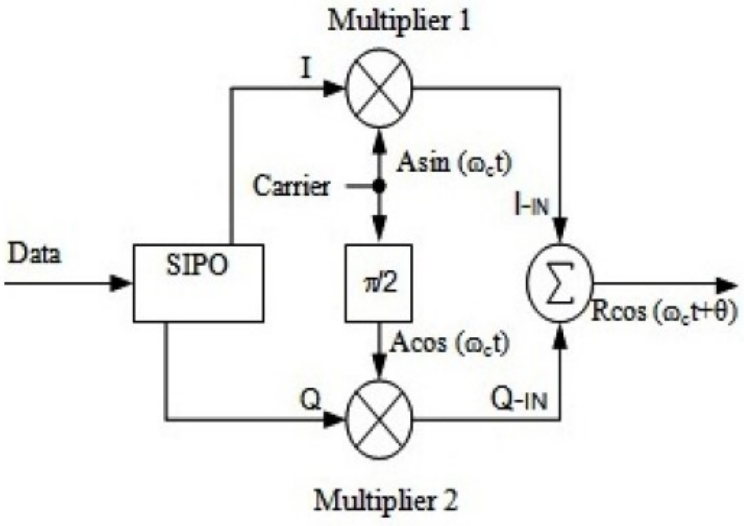

Fig 1. Existing System

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In the existing system, The circuit is based on IQ Modulation. As the symbol contains two bits, so one bit modulates in phase-carrier and second bit will modulate the quadrature phase-carrier. The bits are named as the I and Q respectively, and are transmitted to the modulator via a Serial- In-Parallel-Out (SIPO) shift register. SIPO accepts the input from the data and converts it to the parallel data. The existing system uses two multipliers and the mixer as well so that the circuit area increase and the cost also increase. To avoid this we are using the proposed system.

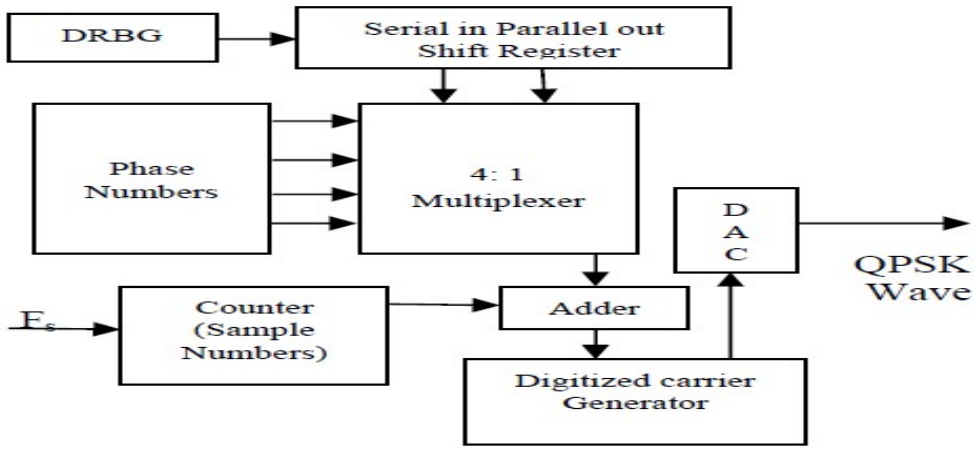

Fig 2. Proposed System

The new approach is proposed for QPSK modulator. In this method the QPSK is generated on the digital platform by means of digitized carrier wave generator. The Proposed circuit does not use the multipliers and mixers but the conventional IQ modulator uses two multipliers, so the proposed circuit minimizes the circuit area as well as cost. We are also adding the parallel processing registers to the proposed system to increase the throughput and the speed.

3. Results and Discussion

3.1 Synthesis Results:

3.1.1 Existing System:

RTL Diagram:

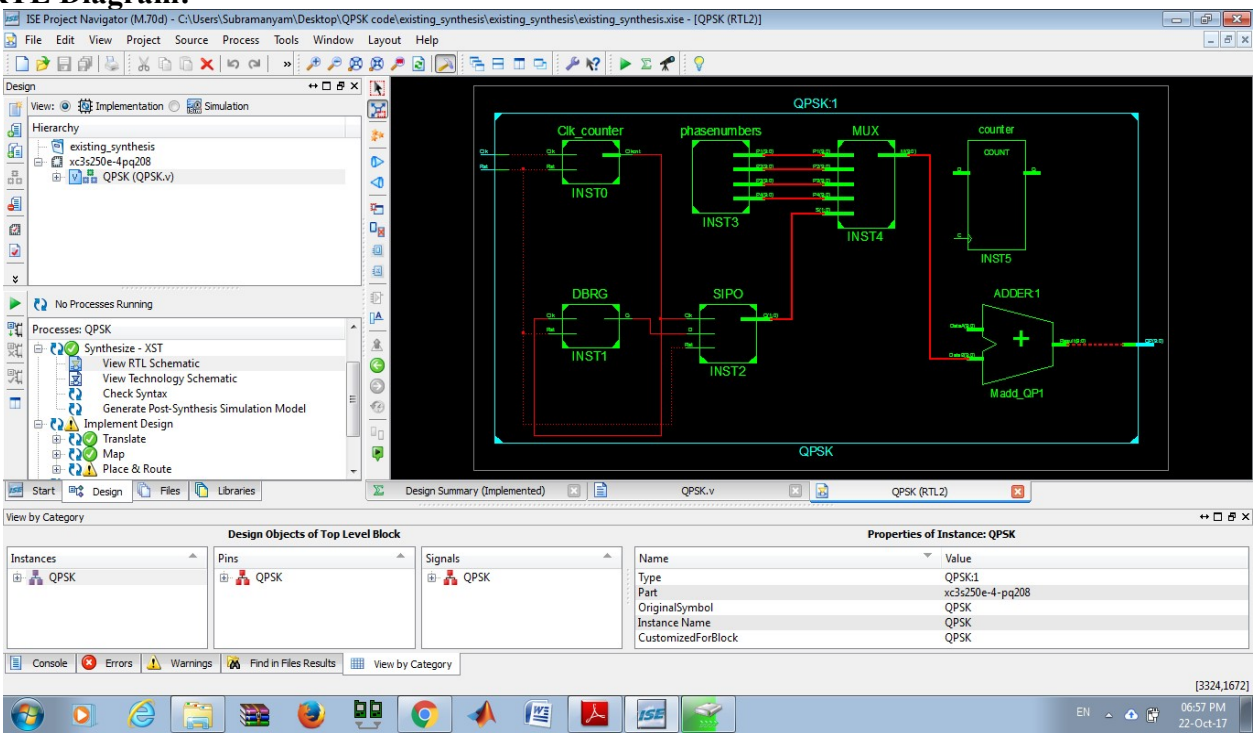

FIG 3: RTL SCHEMATIC DIAGRAM OF THE EXISTING SYSTEMS

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TECHNOLOGY SCHEMATIC DIAGRAM:

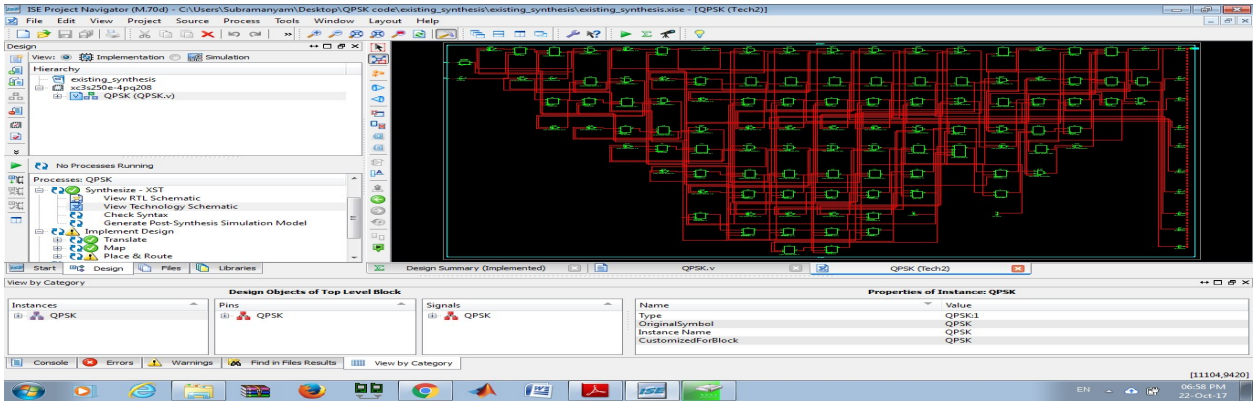

FIG 4: TECHNOLOGY SCHEMATIC DIGRAM OF THE EXISTING SYSTEM

The technology schematic diagram contains the LUTs. Each of the LUT contains a specific function. If the number of Look Up Tables increases then the size of the IC will also increase.

DESIGN SUMMARY:

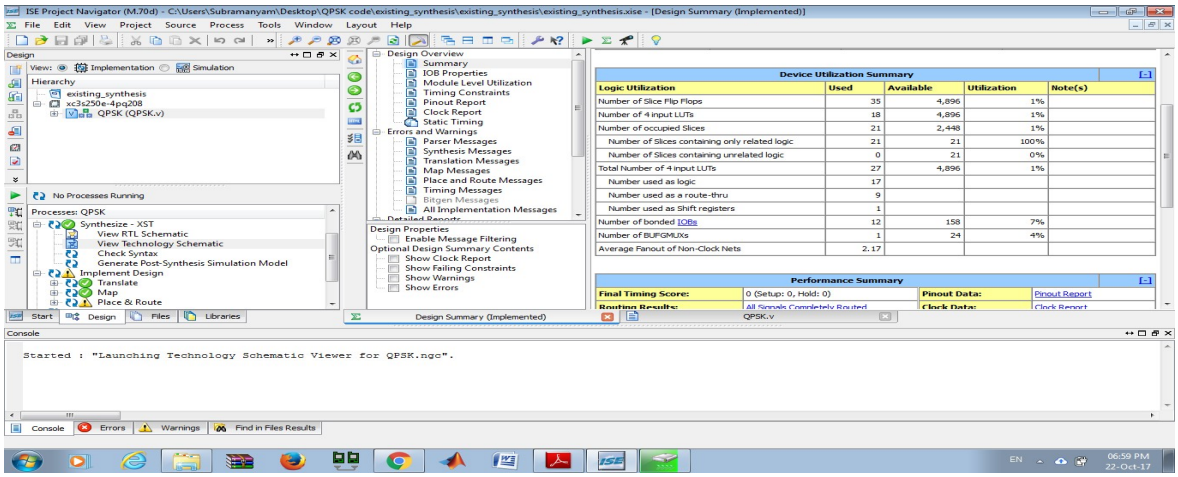

Fig 5: DESIGN SUMMARY OF THE EXISTING SYSTEM

The design summary shows the number of look up tables, number of flip flops and the number of I/O bonds used in the design.

SYNTHESIS REPORT:

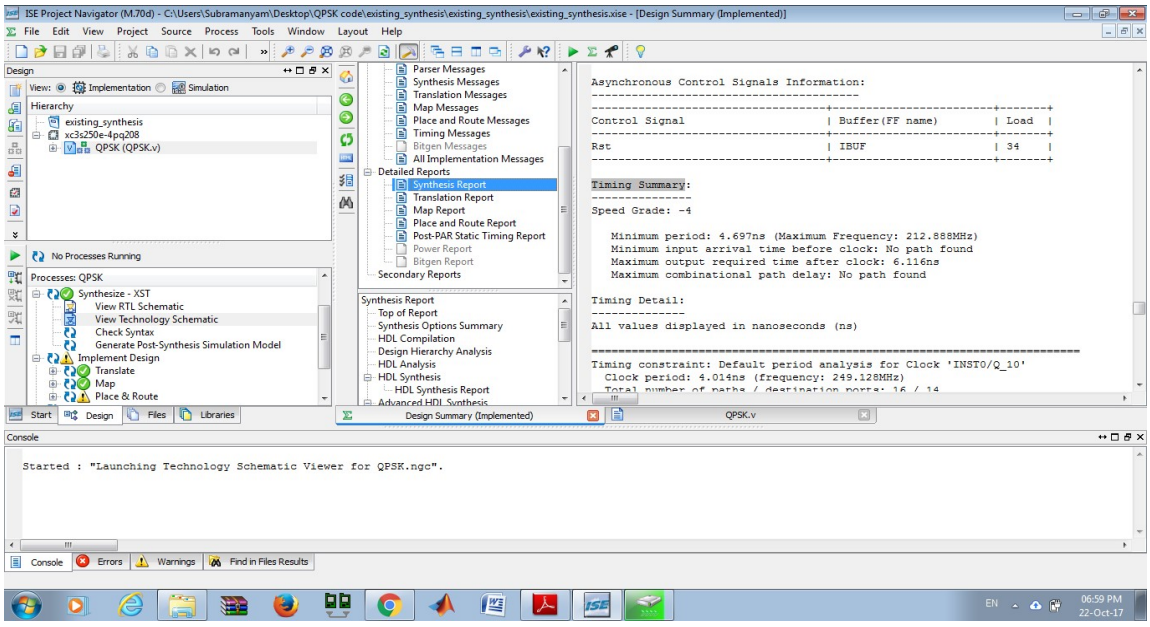

Fig 6: SYNTHESIS REPORT OF THE EXISTING SYSTEM

The synthesis report shows that the delay generated by our design

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3.1.2 PROPOSED SYSTEM:

RTL SCHEMATIC DIAGRAM:

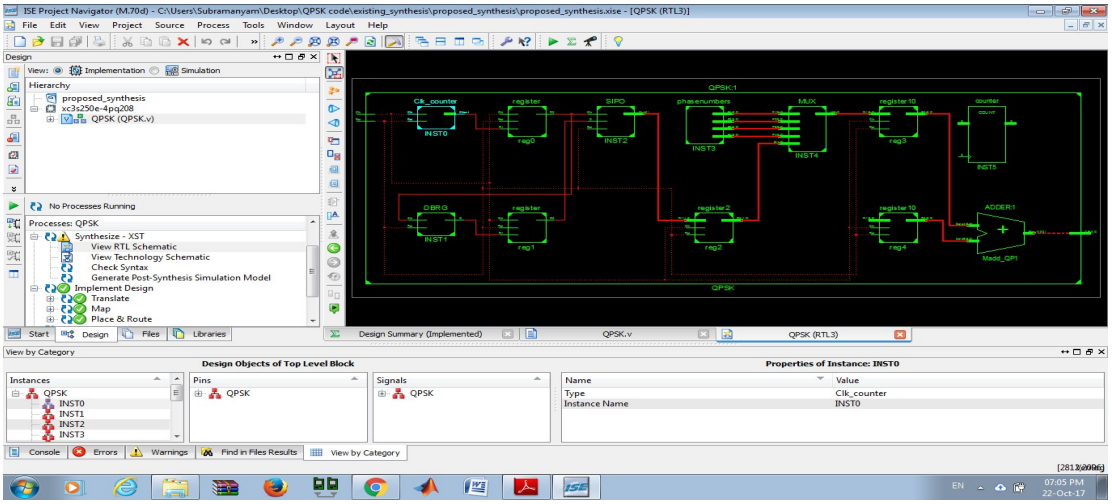

Fig 7: RTL SCHEMATIC DIAGRAM OF THE PROPSOED SYSTEM

SCHEMATIC DIAGRAM:

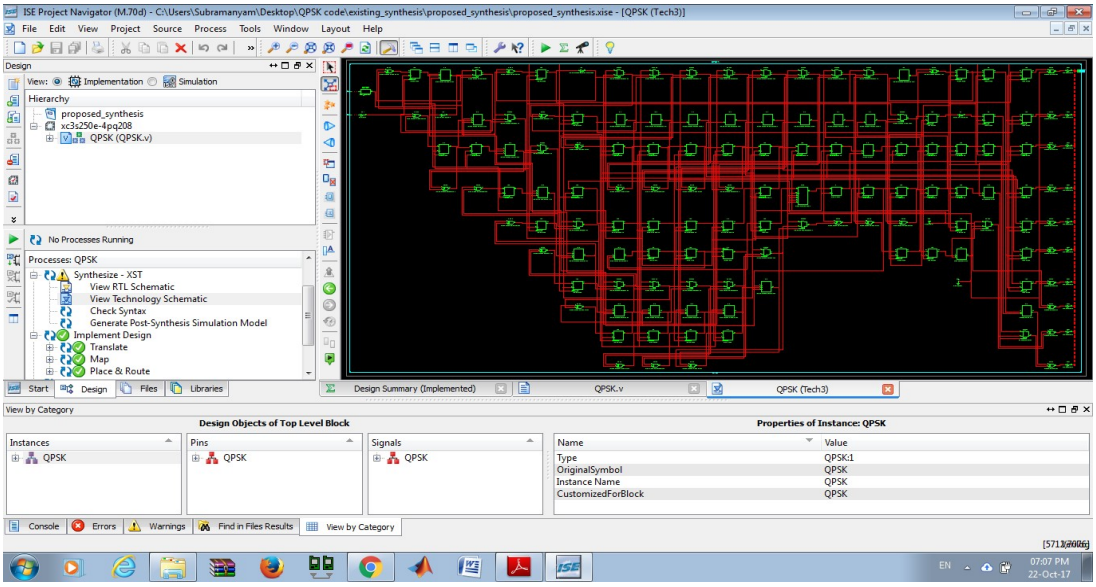

FIG 8: SCHEMATIC DIAGRAM OF THE PROPOSED SYSTEM

DESIGN SUMMARY:

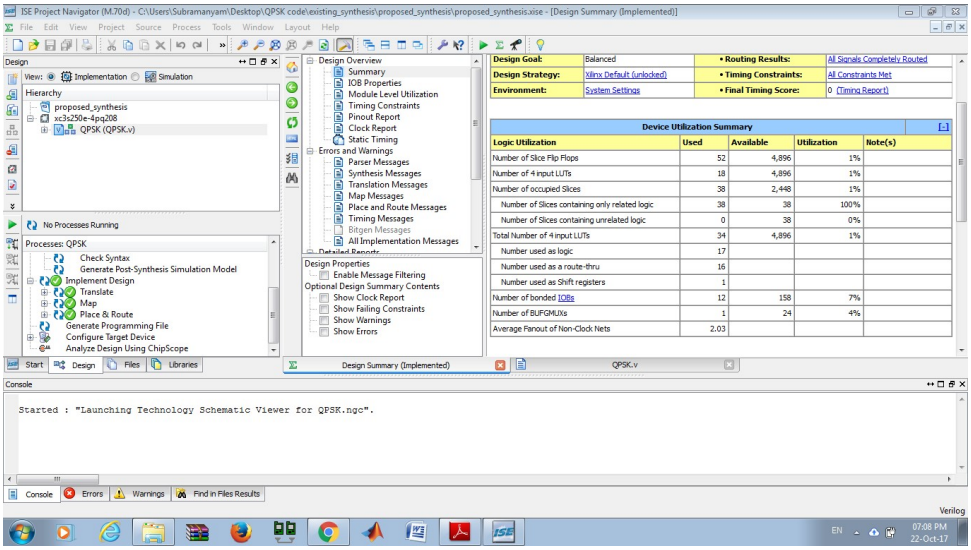

FIG 9: DESIGN SUMMARY OF THE PROPOSED SYSTEM

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SYNTHESIS REPORT:

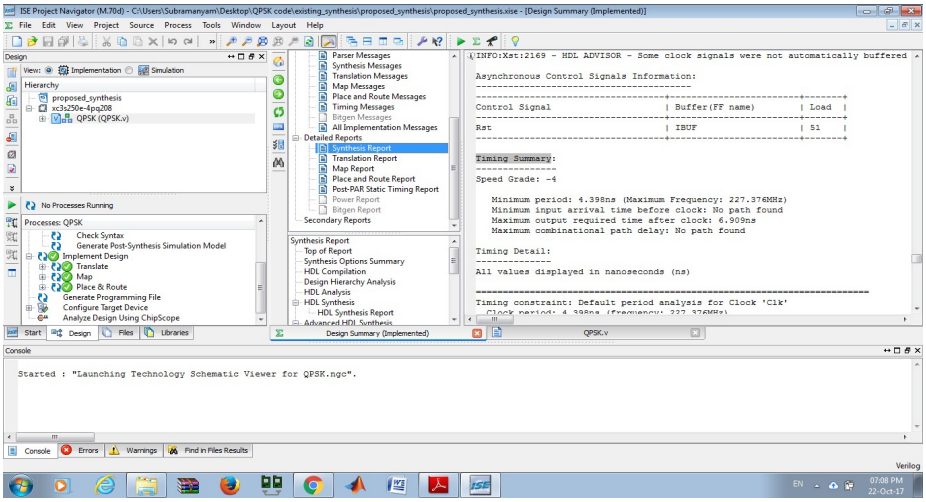

FIG 10: DESIGN SUMMARY OF THE PROPOSED SYSTEM

3.3 SIMULATION RESULTS:

3.3.1 EXISITING SYSTEM:

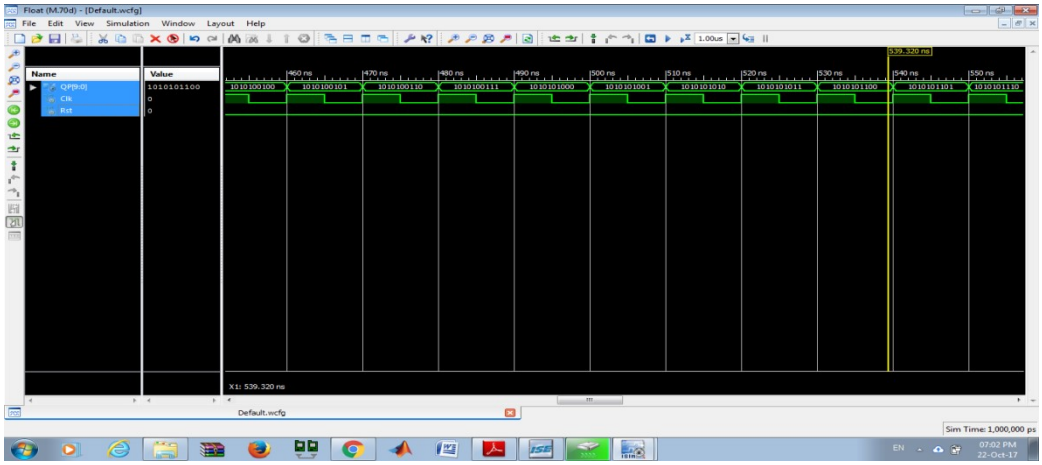

FIG 11: SIMULATION RESULT OF THE EXISTING SYSTEM

3.3.2 PROPOSED SYSTEM:

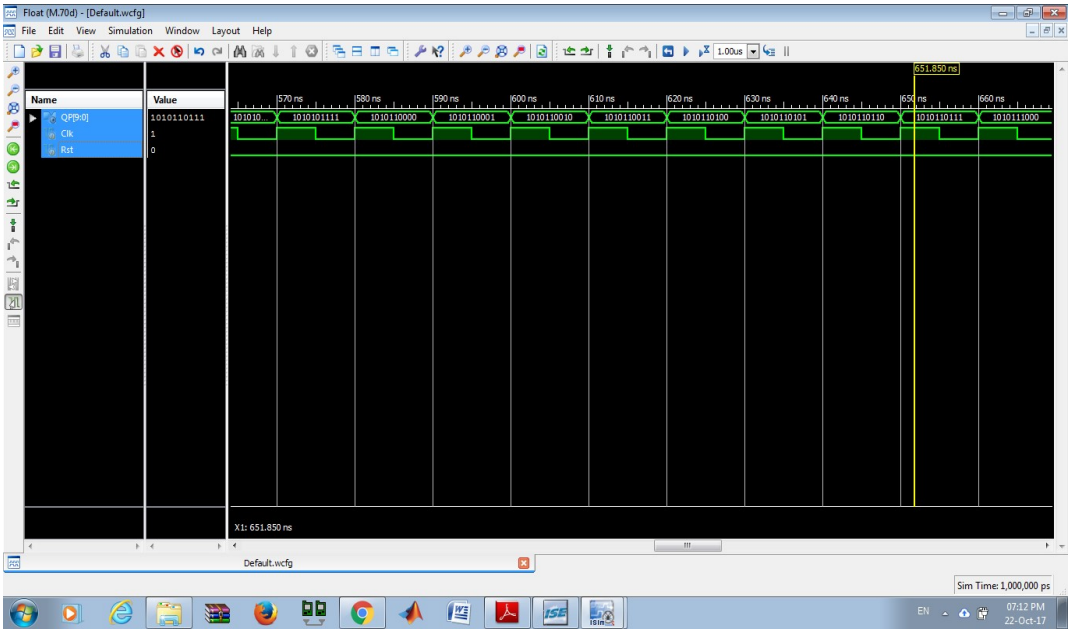

FIG 12: SIMULATION RESULT OF THE PROPSOED SYSTEM

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4. CONCLUSION:

This project presents implementation of the IQ based QPSK Modulator and the proposed digitized QPSK Modulator using Spartan 3E starter Xilinx Board synthesis. Design and implementation as well as for the development of sophisticated digital systems by using Verilog hardware description language.

In this project it is tried to achieve a design for QPSK modulation which will give the same result by minimizing its size or area as well. The reduced delay of the design will reduce the power consumption. The proposed block system, we were used the parallel processing technique to the existing system that will help to increase speed of operation of the design. It means proposed block diagram try to improve all the three main factors power, area, hardware which are taken into consideration for any system design.

FUTURE SCOPE:

In future, we will use the parallel prefix adder in place of the normal adder and also use QCA technology in the design of multipliers to reduce the delay and the area reduction.

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