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Design Of Voltage Level Shifter Using Regulated Cross Coupled Pull Up Networks

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Abstract
Level shifter plays an vital role in multiple supply voltage techniques which creates a path between processors, sensors or broads of different voltage levels, it converts the input logic levels or voltages below the VTH of the transistor to the higher acceptable levels depending upon the system requirements. So, it is necessary to design a level shifter circuit which provides high performance. Power consumption and delay are the key features which determines the performance of a level shifter. This project mainly focuses on designing the level shifter using regulated cross coupled pull up network which helps in utilizing less power and enhancing the speed of the circuit. The work carried out is the mini-project that is a part & parcel of the curriculum in the 2nd semester.
Keywords : Level shifter, Regulated cross coupled (RCC)network, LTspice, Power, Speed.

Introduction

A level shifter, also known as a level converter, logic level shifter, or voltage level translator, is a circuit plays a vital role in digital electronics to translate signals from one logic level or voltage domain to another and even voltages below the VTH of the transistor to the higher acceptable levels depending upon the system requirements. This allows integrated circuits with various voltage requirements, such as TTL and CMOS, to work together. It serves as a bridge between Modern systems such as processors, logic, sensors, and other circuits. the complexity of the system increases with multiple sub-systems, then the system needs multiple power supply voltages to build connection between these sub-blocks. This demands the circuit which converts the voltages as per the system requirement, which is accomplished by level shifter circuit [1]-[5].

Sometimes system may need multiple level shifters this may affect the performance of the system as it is characterized by delay, area, and power utilization. Power dissipation and short-circuit current are diminished by reducing the power supply voltage. When the input and output with different signal levels is connected, the driver's output voltage level may not satisfy the input voltage specifications of receiver and leads to unreliable functioning. This project deals with the design of level shifter which allows compatibility between different blocks of system-on-chip (SoC) designs with different voltage requirements, along with optimized device parameters delay and power dissipation. The CMOS level shifters are typically implemented using either of the two approaches, by using current mirror or Differential cascade voltage switch (DCVS) [6]-[10].

The Fig. 1 shows current mirror-based level shifter, a semi static current mirror is used to limit the current flow, the current is copied from one active node to another. There is no proper beneficial interaction among pull up and pull-down transistor there by strength of the pull up device is weakened when the output node is pulled down by the pull-down device. This diminishes the operational speed and enhances the stand by power due to static current. The Fig. 2 shows the

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current-mirror based Level Shifter. Another common approach is DCVS (differential cascade voltage switch), based on the number of transistors used to design the circuit used they are classified as 6T,8T,10T and advanced level shifter [11]-[15].
8T level shifter is a conventional level shifter shown in Fig 1.2, it is based on DCVS approach includes cross coupled pull up network this rectifies the regenerative interaction, enhances the circuit speed, and absorb less standby power due to absence of static current through the branches. 8T level shifter is suitable only when the value of VDDL is more than VTH, if not then NMOS transistor will be out-phased by PMOS transistor. This disadvantage is taken off by advanced level shifter which consists of more than 10T. In this project an Advanced level shifter with 12T along with regulated cross coupled pull up network is implemented and the tool used for simulation is LTspice 180nm technology and designed in 45nm technology. The presented designs are examined in remarks of delay and power dissipation [16]-[20].

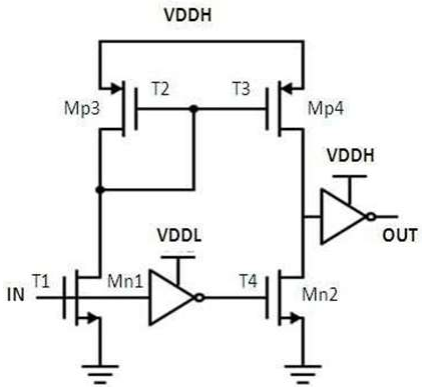

Fig. 1: Current-mirror based Level Shifter.

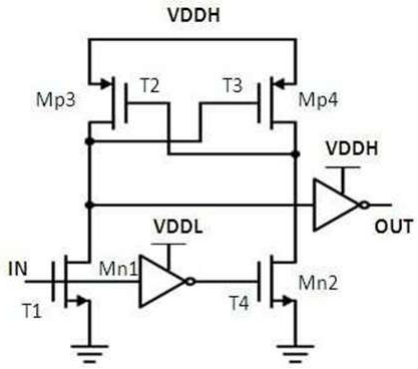

Fig. 2 : Differential Cascade Voltage Switch (DCVS) based level shifter.

Literature survey

In the paper tited, “Rapid Low Power Voltage Level Shifter Utilizing Regulated Cross Coupled Pull Up Network” and authored by N. Arun Vignesh, S. Kanithan, the details are as follows. This paper presents a ultra-low power and high speed voltage or logic level shifter with the help of regulated cross coupled structure in the pull up region the power utilized by the circuit is considerably decreased and speed of the circuit is increased. The LS can convert the input logic level below Vth to higher acceptable levels. A LS requires less area because it consists of a smaller number of components which makes it fit for low power and high-speed applications. Tool used for simulation is LTspice 180nm technology. The level shifter can shift the input voltage or logic level as less as 80mv to higher acceptable levels.
In the paper titled, “A Fast And Low-Power Level Shifter For Multi-Supply Voltage Designs” & authored by Jialu Yin, Jia Yuan, Heng You, Peng Wang, Shushan Qiao, the details are as follows. In this paper, high-speed and ultra-low power level shifter (LS) capable of realizing wide-range voltage level conversion. Two key features are contained in the presented LS to support its superior performances. First, a novel boost control circuit is proposed to boost input voltage and strengthen

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pull-down driven capability, which results in significant improvement of operation speed and conversion range. Second, multi-threshold COMS (MTCMOS) and sub-threshold device sizing techniques are employed to reduce the static current, thereby obtaining ultra-low leakage power consumption. Post-layout simulation results demonstrate that the proposed LS implemented with SMIC 55-nm technology can convert 140 mV low-voltage to 1.2 V

In the paper titled, "Ultra-Low Voltage Level Shifter with Pass Transistor and Reduced-Swing Output Buffer" & authored by Sudhin Sara Kurian, Deepa, the details are as follows. This paper presents an ultra-low voltage level shifter (LS) that converts deep sub-threshold region to the super-threshold region making it well-suited for low-power applications. The proposed LS consummates better performance by addressing the reduced swing and slow fall transition. To attain lower standby power consumption, a novel reduced-swing buffer design is used and a pass transistor is used for bettering the speed of the fall transition. A diode-connected transistor is used to nullify the high static current. Stack approach can be used to further reducing power consumption. The circuit is simulated in a 45-nm process technology and HSPICE is the tool used for the simulation

In the paper titled, "Voltage Level Shifter Circuits in 45nm CMOS Technology - A Review" & authored by Mr. Aneesh A, Mr. Jishnu K Mohanan, Dr. James T G., the details are as follows. This paper demonstrates different voltage level shifter circuits in 45nm CMOS technology. In digital electronics the level shifter is also called as logic level shifter. It is a circuit used to translate signals from one logic level or voltage domain to another logic level or voltage domain. It allows compatibility between different blocks of system-on-chip (SoC) designs with different voltage requirements. The level shifter circuits are compared in terms of voltage shifting level, power dissipation and delay. The input signal is set to 0.3V. The dual supply voltages VDDH is set to 1.1V and VDDL is set to 0.3V. Simulations have been carried out in cadence® EDA tool.

In the paper titled, "A Low-Power and High-Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull-Up Network" & authored by Saideh Kabirpour and Mohsen Jalali, the details are as follows. This paper presents a fast and very low power voltage level shifter (LS) is presented. By using a new regulated cross-coupled (RCC) pull-up network, the switching speed is boosted and the dynamic power consumption is highly reduced. The proposed (LS) has the ability to convert input signals with voltage levels much lower than the threshold voltage of a MOS device to higher nominal supply voltage levels. The presented LS occupies a small silicon area owing to its very low number of elements and is ultra-low-power, making it suitable for low-power applications such as implantable medical devices and wireless sensor networks. Results of the post-layout simulation in a standard 0.18-µm CMOS technology show that the proposed circuit can convert up input voltage levels as low as 80 mV. The power dissipation and propagation delay of the proposed level shifter for a low/high supply voltages of 0.4/1.8 V

Conclusions

The Voltage level shifter using Advanced DCVS differential cascade voltage switch with regulated cross-coupled pull-up network is implemented and simulated in LTspice 180 nm technology and the design is incorporated using 45nm technology, the Voltage level shift from 0.4V to 1.8 V is obtained approaching same delay. The designed voltage level with 45nm technology has optimized delay and an higher voltage when compared with other designs of Level shifter 45nm. The level shift and delay is achieved by varying the device parameter specification.

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