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Design Of Three Stage Comparator Using 90nm Technology

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Abstract
In this paper, the design of three stage comparator using 90nm technology is presented. The comparator is one of the block that limits the speed of the converter, its optimization is crucial and important and design of Analog-to-Digital Converter (ADC),is the speed limiting element in comparator. It describes the schematic design of a three stage CMOS comparator to achieve lower power dissipation and a lower offset voltage, with high-speed operation. Test structure of the comparator are designed using GPDK 90nm. The three-stage comparator makes it possible to use NMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. Simulation results are obtained and it shows that the proposed design can work under 1.8V supply, with an offset voltage of 200mV, and thus, an innovative circuit technique is implemented to overcome these limitations. The work carried out is the mini-project that is a part & parcel of the curriculum in the 2nd semester.

Keywords
Comparator, high speed, Amplification.

Introduction

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. What is meant here by an analog signal is one that can have any of a continuum of amplitude values at a given point in time. In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region.
The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit analog–digital converter. The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into open-loop and regenerative comparators.
The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the

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open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

Figure 1 below shows the circuit symbol for the comparator that will be used . This symbol is identical to that for an operational amplifier, because a comparator has many of the same characteristics as a high-gain amplifier. A positive voltage applied at the VP input will cause the comparator output to go positive, whereas a positive voltage applied at the VN input will cause the comparator output to go negative. The upper and lower voltage limits of the comparator output are defined as VOH and VOL, respectively.

Literature Survey

A number of researchers have worked on the proposed topic & here follows a brief review of the works that are carried out by various authors till date.

In the paper titled, "A three-stage comparator and its modified version with fast speed and low kickback" & authored by Zaoyu Zhuang , Wenzhen Cao, Xizhu Peng, He Tang, the details of the article are as follows. This paper presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the three-stage comparator in this work has an extra amplification stage, which enlarges the voltage gain and increases the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage.

In the paper titled, "Design of three-stage comparator and its modified version using lector technique" & authored by Savita Sonoli Rajashekar V., the details are as follows. This brief presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the three-stage comparator in this work has an extra amplification stage, which enlarges the voltage gain and increases the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification.

In the paper titled, "Voltage comparator with 60% faster speed by using charge pump" & authored by Xiaoxian Liu, Haoyu Zhuang, He Tang, the details are as follows. This brief proposes a novel comparator to greatly increase its comparison speed while not degrading its noise performance. This comparator is well suited for high-speed high-resolution SAR ADCs. Its structure is based on the classic Miyahara's two-stage comparator with the addition of only an extra charge pump. This simple modification greatly accelerates both the second-stage amplification phase and the regeneration phase, leading to significantly increased comparison speed.

In the paper titled, A 1.2-V dynamic bias latch-type comparator in 65-nm cmos with 0.4-mv input noise" & authored by Harijot Singh Bindra, Christiaan Egidius Lokin, Daniel Schinkel, the details are as follows. A latch-type comparator with a dynamic bias pre-amplifier is implemented in a 65nm CMOS process. The dynamic bias with a tail capacitor is simple to implement and ensures that the pre-amplifier output nodes are only partially discharged to reduce the energy consumption. The comparator is analyzed and compared to its prior-art in terms of energy consumption and input referred noise voltage. First-order equations are presented that show how to optimize the pre-amplifier for low noise and high gain. Both the dynamic bias comparator and the prior-art are implemented on the same die and measurements show that the dynamic bias can reduce the average energy consumption by about a factor 2.5 for the same input-equivalent noise at an input common mode level of half the supply voltage.

Like this, a large number of authors have worked on the chosen topic & here, only the important ones which are referred to are presented.

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Simulation Results

The output voltage waveforms of the connected circuit are shown in Fig.6.1. The input voltage is taken as a reference parameter. This parameter is swept from 0 to 1.8V. The reference voltage is taken as 0.5V. Here, the reference voltage is taken as 0.5V.

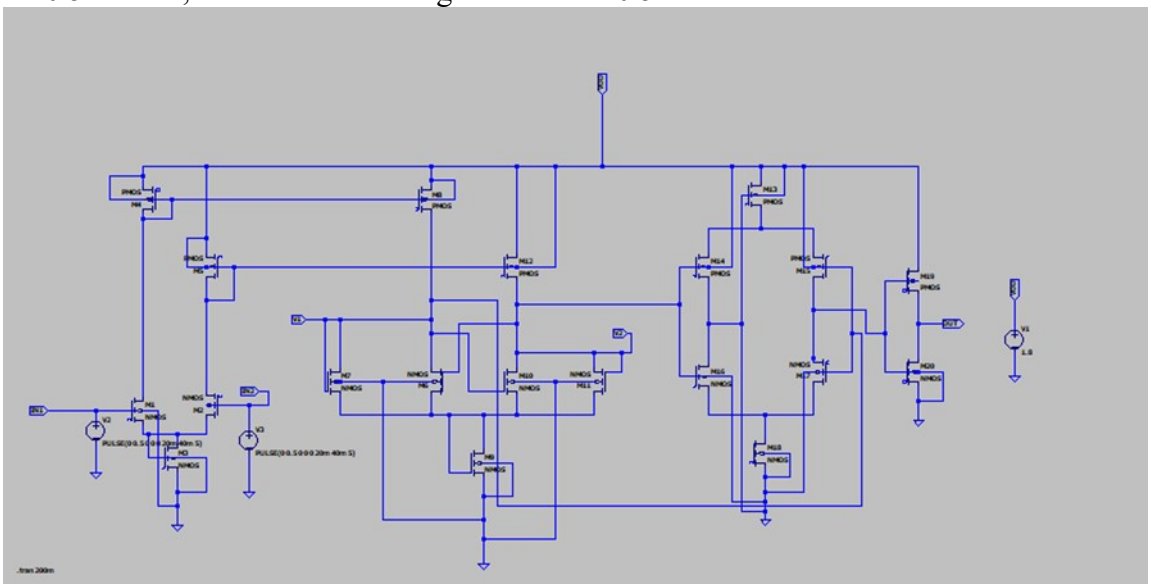

Fig. 1 : Designed circuit

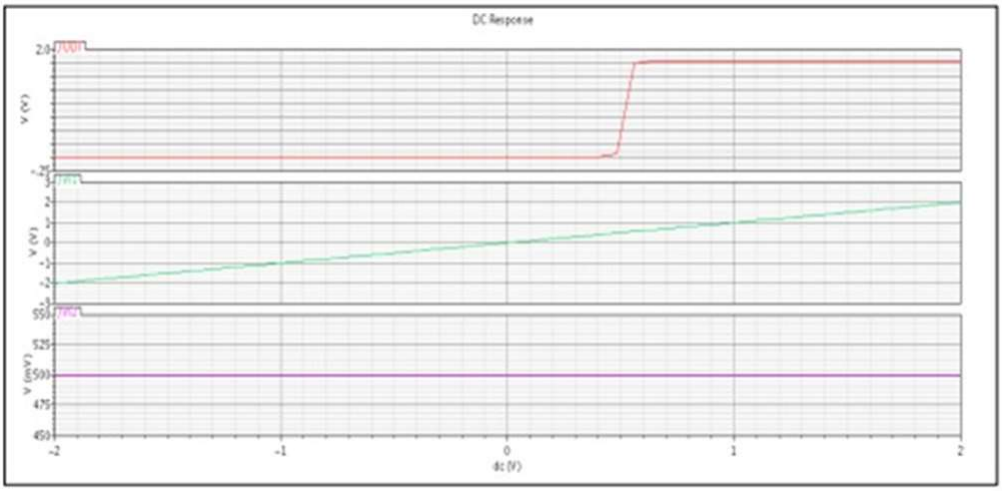

Fig. 2 : Simulated output

Conclusions

In this project, a three stage CMOS comparator topology for low power and high speed applications is presented. A single comparator circuit has been built and tested. The circuit is designed and simulated in GPDK 90nm Technology with LTSPICE simulation environment. Test results are obtained from the test structures designed for different parameters. It shows that the proposed design can work under 1.8V supply, with an offset voltage of 200mV is achieved.

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